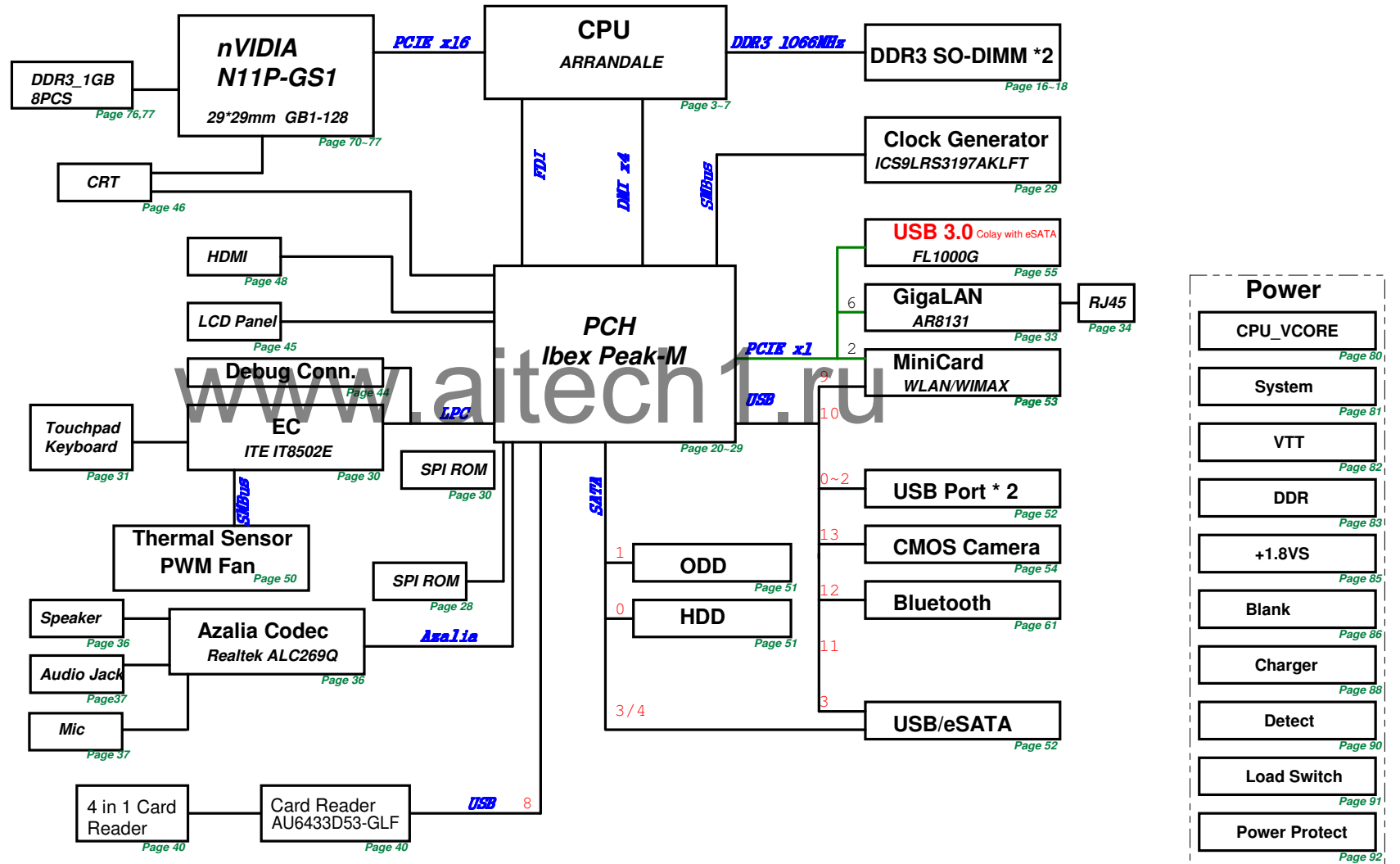


SYSTEM PAGE REF.

01. Block Diagram
02. System Setting
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04. CPU(2)_DDR3
05. CPU(3)_CFG, RSVD, GND
06. CPU(4)_PWR
16. DDR3(1)_SO-DIMM0
17. DDR3(2)_SO-DIMM1
18. DDR3(3)_CA/DQ Voltage
20. PCH(1)_SATA, IHDA, RTC, LPC
21. PCH(2)_PCIE, CLK, SMB, PEG
22. PCH(3)_FDI, DMI, SYS PWR
23. PCH(4)_DP, LVDS, CRT
24. PCH(5)_PCI, NVRAM, USB
25. PCH(6)_CPU, GPIO, MISC
26. PCH(7)_POWER, GND
27. PCH(8)_POWER, GND
28. PCH(9)_SPI, SMB
29. CLK_ICS9LRS3197AKLFT
30. EC_IT8502(1)
31. EC_IT8502(2)KB, TP
32. Reset Circuit
33. LAN_AR8131/8132
34. LAN_RJ45
36. AUD(1)_ALC269Q
37. AUD(2)_MIC, SPK, JACK
40. CB_AU6433 + CardReader
43. CB_NewCard <no NewCard>
44. BUG_Debug
45. CRT(1)_LVDS
46. CRT(2)_D-Sub
48. TV(1)_HDMI
50. FAN_Fan, Thermal Sensor
51. XDD_HDD, ODD
52. USB_USB*3 + eSATA Port
53. MINICARD_WLAN
54. Camera / DMIC
56. LED_Indicator
57. DSG_Discharge
60. DC_DC/BAT CONN
61. BT_Bluetooth
63. FP_Option
65. ME_CONN, Skew Hole
68. OTH_Small BD
70. VGA(1)
71. VGA(2)
72. VGA(3)
73. VGA(4)
74. VGA(5)
75. VGA(6)
76. VGA(7)
77. VGA(8)
78. VGA(9)
80. PWR(1)_VCORE
81. PWR(2)_SYSTEM
82. PWR(3)_+1.1VS_VGA/1.05VS
83. PWR(4)_DDR & +VTT_CPU
85. PWR(6)_+1.8VS & +0.75VS
86. PWR(7)_+VGF_X_CORE_Remove
87. PWR(8)_+VGA_CORE
88. PWR(9)_CHARGER
90. PWR(11)_DETECT
91. PWR(12)_LOAD SWITCH
92. PWR(13)_PROTECT
93. PWR(14)_SIGNAL
94. PWR(15)_FLOWCHART

H54FE Capella Platform Non-iAMT Rev. 1.1 BLOCK DIAGRAM 2010-05-13



PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	-	-	-	+3VS
GPIO 01	-	-	INT TBD	+3VS
GPIO [2:5]	-	-	EXT PU	+5VS
GPIO 06	-	-	INT TBD	+3VS
GPIO 07	-	-	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	-	-	EXT PU	+3VSUS
GPIO 10	-	-	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	LAN_PHY_PWR_CTRL	EXT PU	+3VSUS
GPIO 13	-	-	-	+3VSUS
GPIO 14	-	-	EXT PU	+3VSUS
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS
GPIO 16	-	-	-	+3VS
GPIO 17	GPO	WLAN_LED	EXT PD & INT TBD	+3VS
GPIO 18	Native	PCIECLKRQ1#	EXT PU	+3VS
GPIO 19	-	-	-	+3VS
GPIO 20	Native	PCIECLKRQ2#	EXT PU	+3VS
GPIO 21	-	-	-	+3VS
GPIO 22	GPI	BT_DET#	EXT PU	+3VS
GPIO 23	-	-	INT PU	+3VS
GPIO 24	-	-	-	+3VSUS
GPIO 25	Native	PCIECLKRQ3#	EXT PU	+3VSUS
GPIO 26	-	-	EXT PU (Not used)	+3VSUS
GPIO 27	GPO	BT_ON	INT WEAK PU	+3VSUS
GPIO 28	GPO	BT_LED	EXT PD	+3VSUS
GPIO 29	Native	SLP_LAN#	-	+3VSUS
GPIO 30	Native	SUS_PWR_ACK	-	+3VSUS
GPIO 31	Native	ACPRESENT	-	+3VSUS
GPIO 32	Native	CLKRUN#	-	+3VS
GPIO 33	-	-	-	+3VS
GPIO 34	Native	STP_PCI#	-	+3VS
GPIO 35	-	-	-	+3VS
GPIO 36	-	-	-	+3VS
GPIO 37	GPI	PCB_ID0/SPIROM_ID0	EXT PD	+3VS
GPIO 38	GPI	PCB_ID1/SPIROM_ID1	EXT PD	+3VS
GPIO 39	GPI	PCB_ID2	EXT PD	+3VS
GPIO 40	-	-	EXT PU (Not used)	+3VSUS
GPIO 41	-	-	EXT PU (Not used)	+3VSUS
GPIO 42	-	-	EXT PU (Not used)	+3VSUS
GPIO 43	-	-	EXT PU (Not used)	+3VSUS
GPIO 44	-	-	EXT PU (Not used)	+3VSUS
GPIO 45	-	-	EXT PU (Not used)	+3VSUS
GPIO 46	-	-	EXT PU (Not used)	+3VSUS
GPIO 47	Native	PEG_A_CLKRQ#	EXT PD	+3VSUS
GPIO 48	-	-	-	+3VS
GPIO 49	-	-	-	+3VS
GPIO 50	-	-	EXT PU (Not used)	+5VS
GPIO 51	-	-	INT PU	+3VS
GPIO 52	-	-	-	+5VS
GPIO 53	-	-	INT PU	+3VS
GPIO 54	-	-	-	+5VS
GPIO 55	-	-	INT PU	+3VS
GPIO 56	Native	PEG_B_CLKRQ#	EXT PU	+3VSUS
GPIO 57	-	-	-	+3VSUS
GPIO 58	Native	SML1CLK	-	+3VSUS
GPIO 59	-	-	EXT PU (Not used)	+3VSUS
GPIO 60	-	-	-	+3VSUS
GPIO 61	-	-	-	+3VSUS
GPIO 62	-	-	-	+3VSUS
GPIO 63	-	-	-	+3VSUS
GPIO 64	Native	CLKOUTFLEX0	INT TBD	+3VS
GPIO 65	Native	CLKOUTFLEX1	INT TBD	+3VS
GPIO 66	-	-	INT TBD	+3VS
GPIO 67	-	-	INT TBD	+3VS
GPIO 72	-	-	-	+3VSUS
GPIO 73	-	-	EXT PU (Not used)	+3VSUS
GPIO 74	-	-	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1DATA	-	+3VSUS

EC-it8502	Signal Name
GPA0	PWR_LED_UP#
GPA1	CHG_LED_UP#
GPA2	BATSEL_3S#
GPA3	DEEP_IDLE
GPA4	LCD_BL_PWM
GPA5	FAN_PWM
GPA6	BAT1_CNT1#
GPA7	BAT2_CNT1#
GPB0	CHG_EN#
GPB1	PRECHG
GPB2	CTX0
GPB3	SMB0_CLK
GPB4	SMB0_DAT
GPB5	A20GATE
GPB6	RCIN#
GPB7	PM_RSMRST#
GPC0	CIR_RX
GPC1	SMB1_CLK
GPC2	SMB1_DAT
GPC3	PM_PWRBTN#
GPC4	AC_IN_OC#
GPC5	OP_SD#
GPC6	BAT1_IN_OC#
GPC7	RFON_SW#
GPD0	PWRLIMIT#
GPD1	PM_SUSC#
GPD2	BUF_PLT_RST#
GPD3	EXT_SCI#
GPD4	EXT_SMI#
GPD5	LCD_BACKOFF#
GPD6	FAN0_TACH
GPD7	COLOREN#
GPE0	VSUS_ON
GPE1	SUSC_EC#
GPE2	SUSB_EC#
GPE3	CPU_VRON
GPE4	PWR_SW#
GPE5	BAT2_IN_OC#
GPE6	LID_SW#
GPE7	CAP_ACK#
GPF0	HDMI_HPD
GPF1	WLAN_SW#
GPF2	PS2CLK1
GPF3	TP_SW#
GPF4	TP_CLK
GPF5	TP_DAT
GPF6	THRO_CPU
GP7	
GP8	
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GP11	
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GP99	

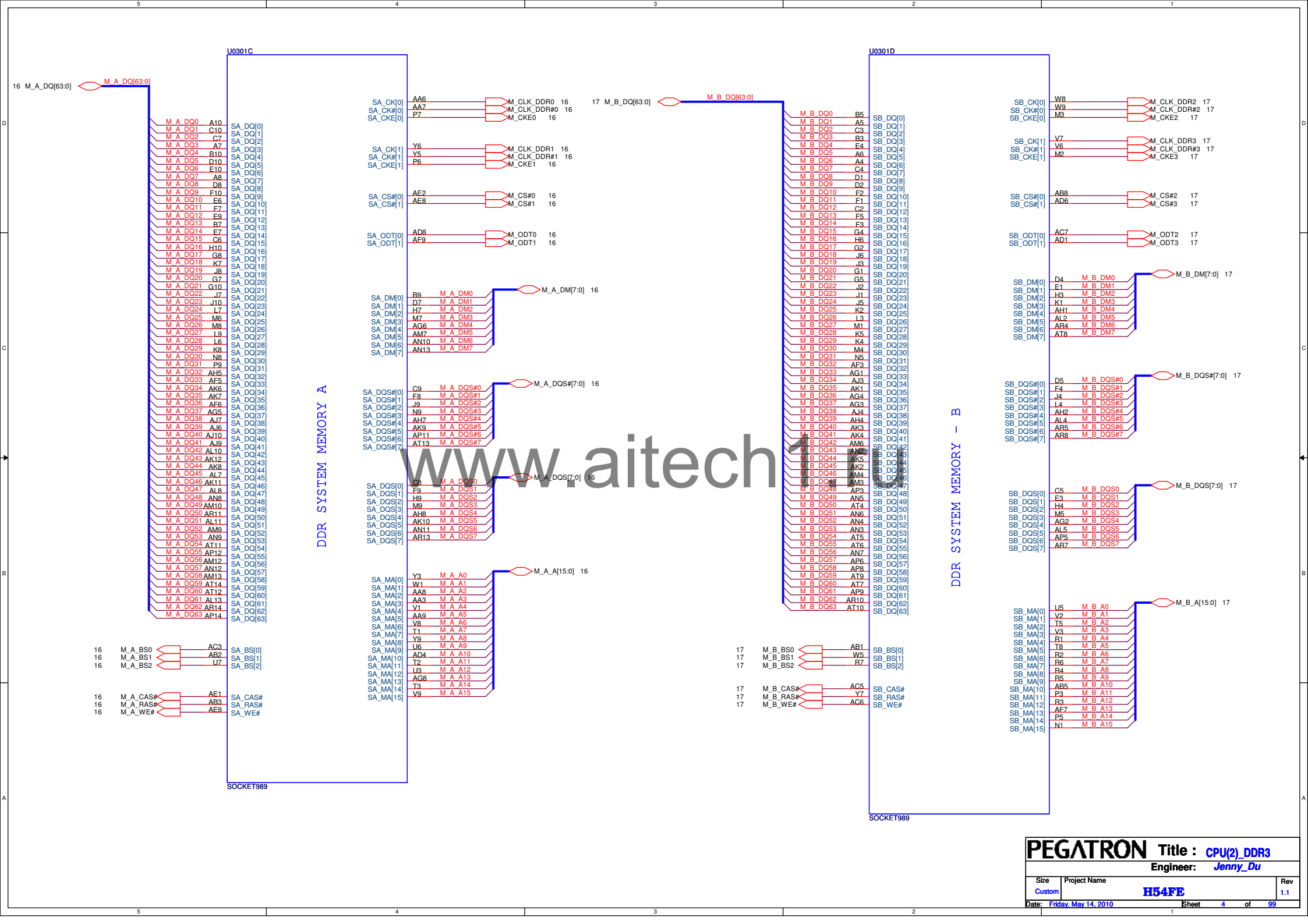
SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2h)
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)
CPU Thermal IC(G780)	1001100x (98h)
VGA Thermal IC(G781-1)	1001101x (9Ah)
VGA Thermal Sensor(NB9E-GE1)	1001111x (9Eh)
VID Controller ASM8272	0011011x (36h)
DSP FM2010	

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	N/A
PCIE 5	PCIE to SATA (SR)
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD(1)
SATA1	SATA ODD
SATA2	N/A
SATA3	N/A
SATA4	SATA HDD(2)
SATA5	eSATA

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	CMOS Camera
USB 5	Newcard
USB 6	Minicard TV Tuner
USB 7	N/A
USB 8	OLED
USB 9	WLAN
USB 10	N/A
USB 11	USB Port (5)
USB 12	Bluetooth
USB 13	Finger Print



U0301E

AP25
AL25
AL24
AL22
AJ33
AG9
M27
J28
J17
H17
G17
E31
E30

10mil trace

18 DIMM0_VREF_DQ
18 DIMM1_VREF_DQ

T0538 1 CFG0 AM30
T0527 1 CFG1 AM28
T0526 1 CFG2 AP31
T0525 1 CFG3 AL32
T0529 1 CFG4 AL30
T0528 1 CFG5 AM31
T0531 1 CFG6 AN33
T0532 1 CFG7 AM32
T0534 1 CFG8 AK32
T0530 1 CFG9 AK31
T0535 1 CFG10 AK28
T0533 1 CFG11 AJ28
T0536 1 CFG12 AN30
T0537 1 CFG13 AN32
T0543 1 CFG14 AJ32
T0541 1 CFG15 AJ29
T0540 1 CFG16 AJ30
T0539 1 CFG17 AK30
T542 1 CFG18 H16

RSVD_TP_86

B19
A19

U9
T9

AC9
AB9

T0513 1 C1
T0510 1 A3

RSVD_NCTF_23
RSVD_NCTF_24

J29
J28

T0511 1 A34
T0512 1 A33

RSVD_NCTF_28
RSVD_NCTF_29

T0514 1 C35
T0515 1 B35

RSVD_NCTF_30
RSVD_NCTF_31

SOCKET989

RESERVED

RSVD32 AJ13 1 T0517
RSVD33 AJ12 1 T0506
RSVD34 AH25 1 T0519
RSVD35 AK26 1 T0520
RSVD36 AL26 1 T0504
RSVD_NCTF_37 AR2 1
RSVD38 AJ26
RSVD39 AJ27
RSVD_NCTF_40 AP1 1 T0501
RSVD_NCTF_41 AT2 1 T0518
RSVD_NCTF_42 AT3 1 T0507
RSVD_NCTF_43 AR1 1 T0503

RSVD45 AL28
RSVD46 AL25
RSVD47 AP30
RSVD48 AP32
RSVD49 AL27
RSVD50 AT31
RSVD51 AT32
RSVD52 AB33
RSVD53 AT33 1 T0508
RSVD_NCTF_54 AT34 1 T0509
RSVD_NCTF_55 AP35 1 T0502
RSVD_NCTF_56 AR35 1 T0505
RSVD58 AR32

RSVD_TP_59 E15
RSVD_TP_60 F15
KEY A2
D15
RSVD62 C15
RSVD63 AJ15
RSVD64 SP0503 2
RSVD65 AH15
RSVD65 SP0504 2

RSVD_TP_66 AA5
RSVD_TP_67 AA4
RSVD_TP_68 AB5
RSVD_TP_69 AD5
RSVD_TP_70 AJ5
RSVD_TP_71 AJ5
RSVD_TP_72 AA1
RSVD_TP_73 AH34
RSVD_TP_74 AG1
RSVD_TP_75 AE3

RSVD_TP_76 V4
RSVD_TP_77 V5
RSVD_TP_78 N2
RSVD_TP_79 AD5
RSVD_TP_80 AD7
RSVD_TP_81 W3
RSVD_TP_82 W2
RSVD_TP_83 N3
RSVD_TP_84 AE5
RSVD_TP_85 AD9

VSS

U0301H

AT20 VSS1
AT17 VSS2
AR31 VSS3
AR28 VSS4
AR26 VSS5
AR24 VSS6
AR20 VSS7
AR17 VSS8
AR15 VSS9
AR12 VSS10
AR9 VSS11
AR6 VSS12
AR3 VSS13
AP20 VSS14
AP17 VSS15
AP13 VSS16
AP10 VSS17
AP7 VSS18
AP4 VSS19
AP2 VSS20
VSS21
AN34 VSS22
AN31 VSS23
AN23 VSS24
AN20 VSS25
AN17 VSS26
AM29 VSS27
AM27 VSS28
AM25 VSS29
AM20 VSS30
AM14 VSS31
AM11 VSS32
AM8 VSS33
AM5 VSS34
AM2 VSS35
AL34 VSS36
AL31 VSS37
AL23 VSS38
AL19 VSS39
AL20 VSS40
AL17 VSS41
AL12 VSS42
AL9 VSS43
AL6 VSS44
AL3 VSS45
VSS46
AK29 VSS46
AK27 VSS47
AK25 VSS48
AK20 VSS49
AK17 VSS50
AJ31 VSS51
AJ23 VSS52
AJ20 VSS53
AJ17 VSS54
AJ14 VSS55
AJ11 VSS56
AJ8 VSS57
AJ5 VSS58
AJ2 VSS59
AH35 VSS60
AH34 VSS61
AH33 VSS62
AH32 VSS63
AH31 VSS64
VSS65
VSS66
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VSS79
VSS80

VSS

VSS81 AE34
VSS82 AE33
VSS83 AE32
VSS84 AE31
VSS85 AE30
VSS86 AE29
VSS87 AE28
VSS88 AE27
VSS89 AE26
VSS90 AE6
VSS91 AD10
VSS92 AC2
VSS93 AC4
VSS94 AC2
VSS95 AB35
VSS96 AB34
VSS97 AB33
VSS98 AB32
VSS99 AB31
VSS100 AB30
VSS101 AB29
VSS102 AB28
VSS103 AB27
VSS104 AB26
VSS105 AB6
VSS106 Y8
VSS107 Y8
VSS108 Y4
VSS109 Y2
VSS110 W2
VSS111 W3
VSS112 W3
VSS113 W3
VSS114 W3
VSS115 W3
VSS116 W2
VSS117 W2
VSS118 W2
VSS119 W2
VSS120 W6
VSS121 V10
VSS122 U8
VSS123 U4
VSS124 U2
VSS125 T35
VSS126 T34
VSS127 T33
VSS128 T32
VSS129 T31
VSS130 T30
VSS131 T29
VSS132 T28
VSS133 T27
VSS134 T26
VSS135 T25
VSS136 T24
VSS137 T23
VSS138 T22
VSS139 P8
VSS140 P4
VSS141 P2
VSS142 N35
VSS143 N34
VSS144 N33
VSS145 N32
VSS146 N31
VSS147 N29
VSS148 N28
VSS149 N27
VSS150 N26
VSS151 M10
VSS152 L35
VSS153 L32
VSS154 L29
VSS155 L8
VSS156 L5
VSS157 L2
VSS158 K34
VSS159 K33
VSS160 K30

U0301I

K27
VSS161
VSS162 K9
VSS163 K6
VSS164 K3
VSS165 J32
VSS166 J30
VSS167 J21
VSS168 J19
VSS169 H35
VSS170 H32
VSS171 H28
VSS172 H26
VSS173 H24
VSS174 H22
VSS175 H18
VSS176 H15
VSS177 H11
VSS178 H8
VSS179 H5
VSS180 H2
VSS181 G34
VSS182 G31
VSS183 G20
VSS184 G9
VSS185 G6
VSS186 G3
VSS187 F30
VSS188 F27
VSS189 F25
VSS190 F22
VSS191 F19
VSS192 F16
VSS193 F15
VSS194 F12
VSS195 E29
VSS196 E24
VSS197 E21
VSS198 E18
VSS199 E15
VSS200 E11
VSS201 E8
VSS202 E5
VSS203 E2
VSS204 D33
VSS205 D30
VSS206 D26
VSS207 D9
VSS208 D6
VSS209 D3
VSS210 C34
VSS211 C32
VSS212 C29
VSS213 C28
VSS214 C24
VSS215 C22
VSS216 C20
VSS217 C19
VSS218 C16
VSS219 B31
VSS220 B25
VSS221 B21
VSS222 B18
VSS223 B17
VSS224 B13
VSS225 B11
VSS226 B8
VSS227 B6
VSS228 B4
VSS229 A29
VSS230 A27
VSS231 A23
VSS232 A9
VSS233

VSS

NCTF

VSS_NCTF1 AT35 TP VSS NCTF1 1 T0524
VSS_NCTF2 AT1 TP VSS NCTF2 1 T0521
VSS_NCTF3 AB34
VSS_NCTF4 B34
VSS_NCTF5 B2
VSS_NCTF6 B1 TP VSS NCTF6 1 T0523
VSS_NCTF7 A35 TP VSS NCTF7 1 T0522

SOCKET989

CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)

- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

CFG[3]: PCIe Static Numbering Lane Reversal.(Auburndale Only)

- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed '15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Auburndale Only)

- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

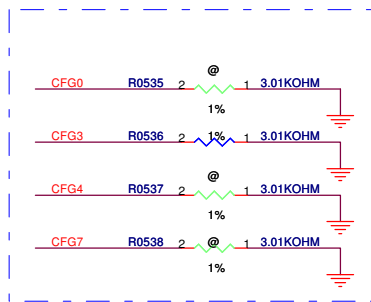
CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)

Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.
For a common motherboard design (for AUB and CFD),the pull-down resistor should be used. Does not impact AUB functionality.

Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

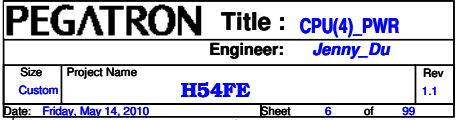
Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



PEGATRON Title : CPU(3)_CFG_GND

Engineer: Jenny_Du

Size	Project Name	Rev
Custom	H54FE	1.1
Date: Friday, May 14, 2010	Sheet 5 of 99	

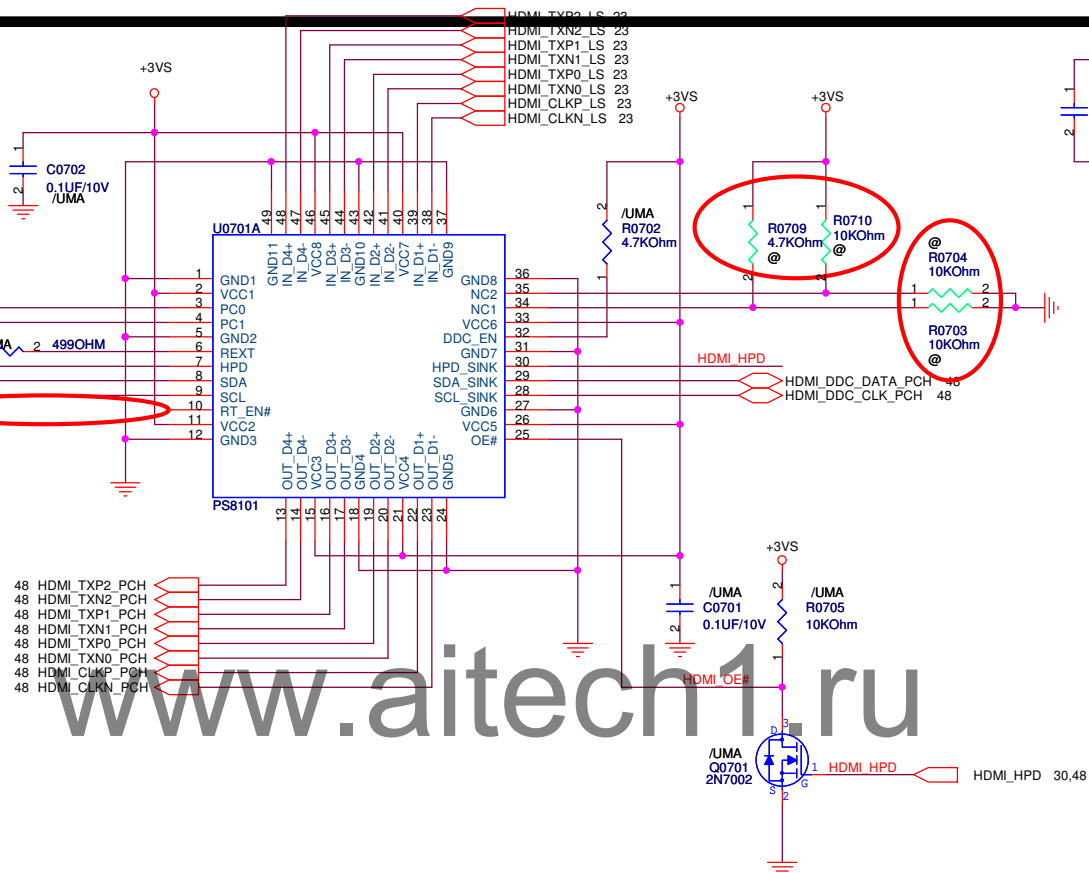


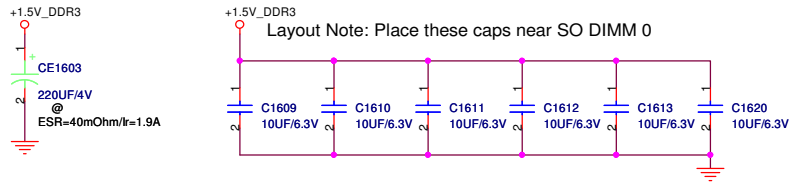
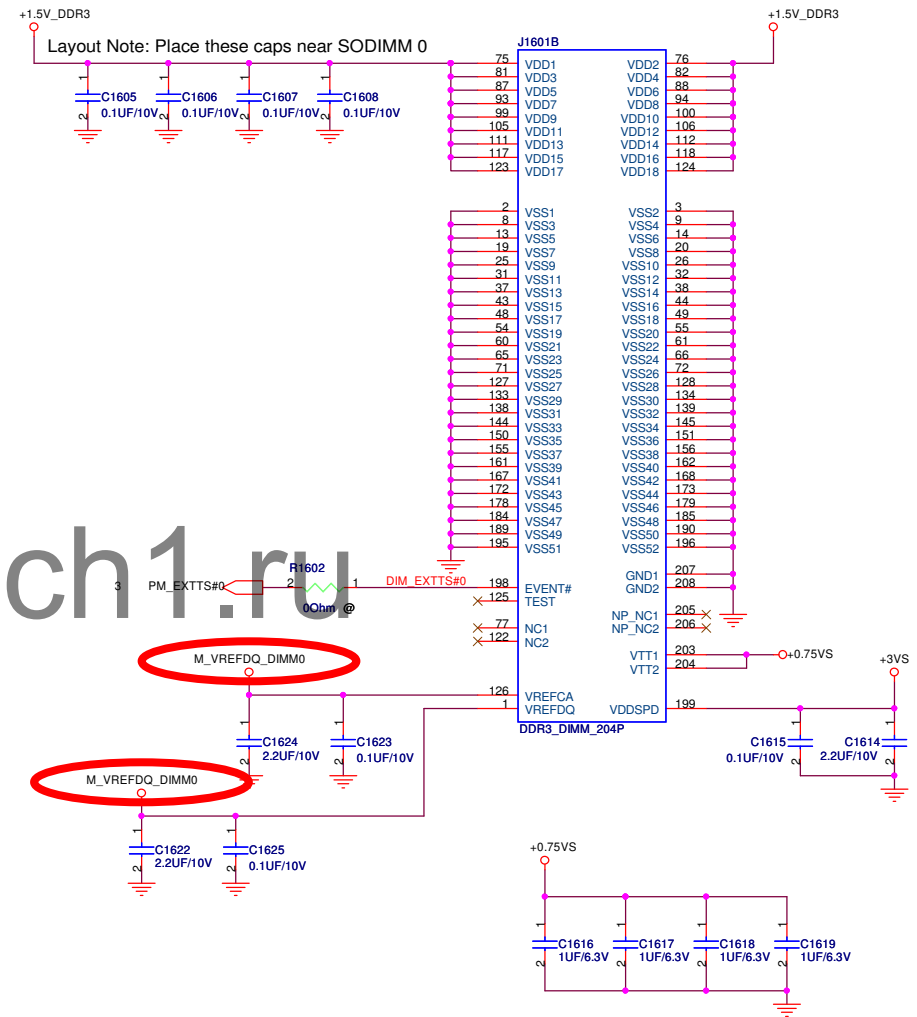
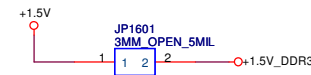
TMDs inputs equalization control.
Internal pull-up at 500K ohm.

PC1	PC0	
0	0	8dB
0	1	4dB
1	0	12dB
1	1	0dB

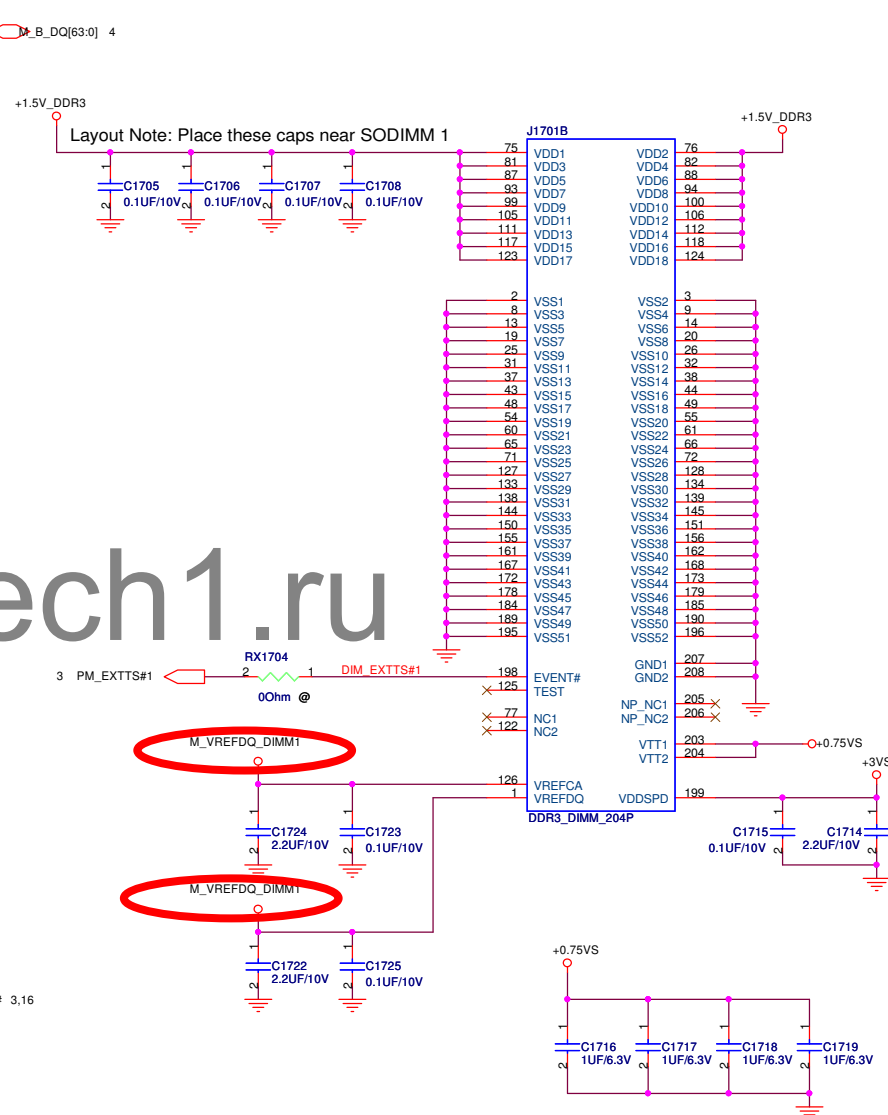
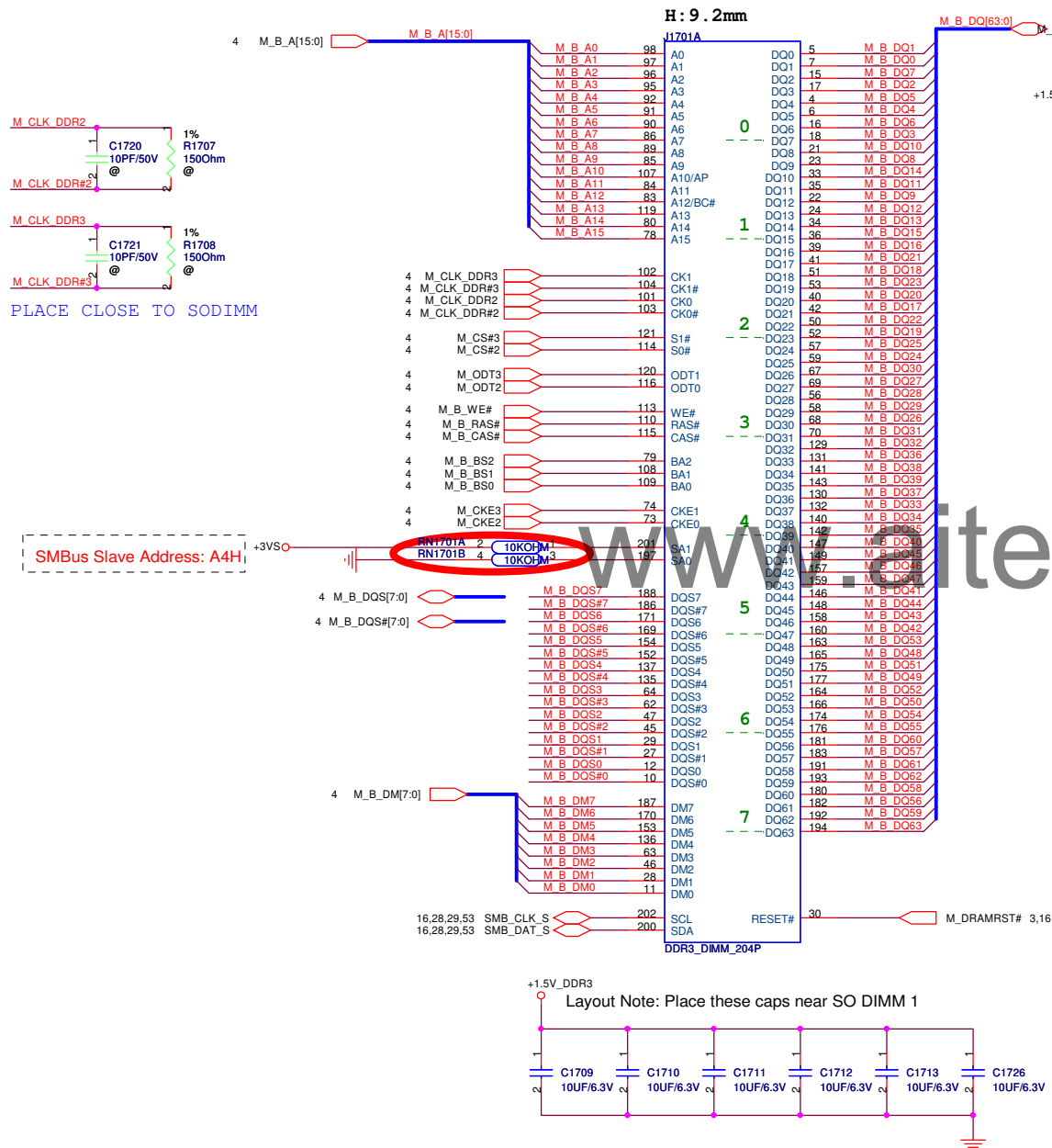
HPD# output voltage configuration

CFG1	CFG0	Voh of HDP#
0	0	0.9V
0	1	0.8V
1	0	1.0V
1	1	External pull-up resistor, Voh is determined by external supply.



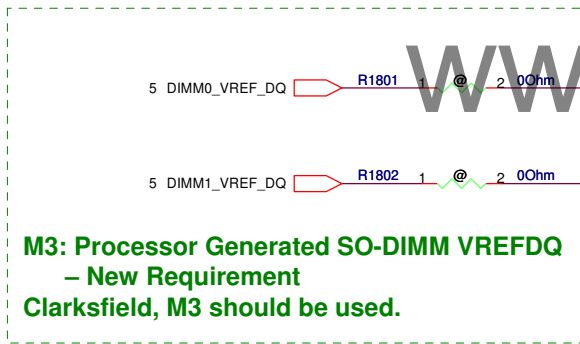
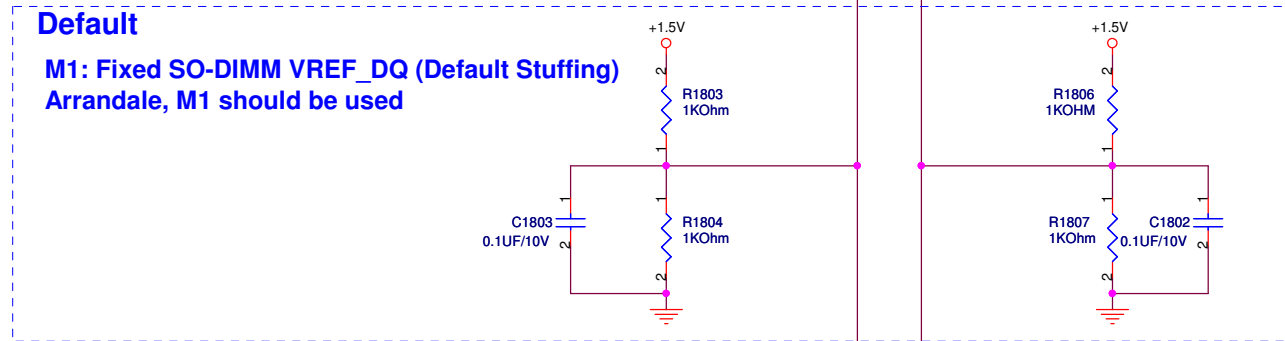


+1.5V +1.5V 3,6,16,18,57,83,91
+1.5V_DDR3 +1.5V_DDR3 16
+0.75VS +0.75VS 16,18,57,83
+3VS +3VS 3,7,16,20,21,22,23,24,25,26,27,28,29,30,32,36,37,44,45,46,48,50,51,53,54,56,57,80,86,87,91,92
M_VREFDQ_DIMM1 M_VREFDQ_DIMM1 16,18



DDR3 Vref

+0.75VS		+0.75VS	16,17,57,83
+1.5V		+1.5V	3,6,16,57,83,91
M_VREFDQ_DIMM0		M_VREFDQ_DIMM0	16,17
M_VREFDQ_DIMM1		M_VREFDQ_DIMM1	16,17

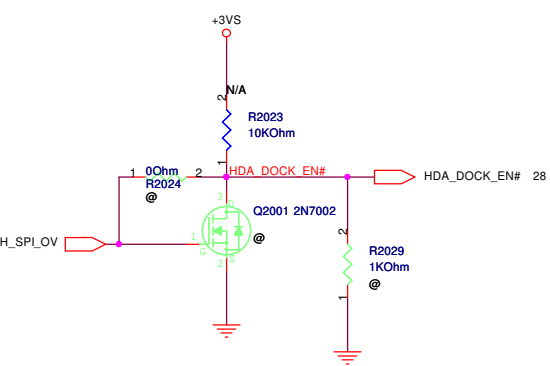
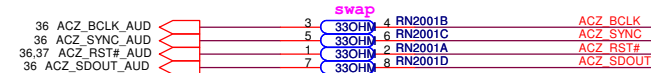


Design Guidelines P.104
板子回來再check

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

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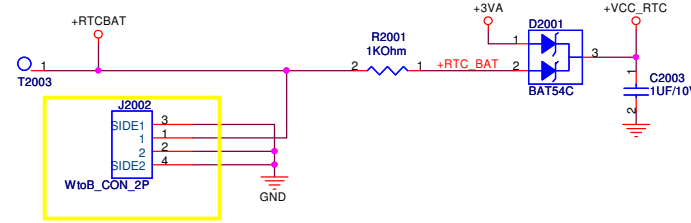


Strap information:

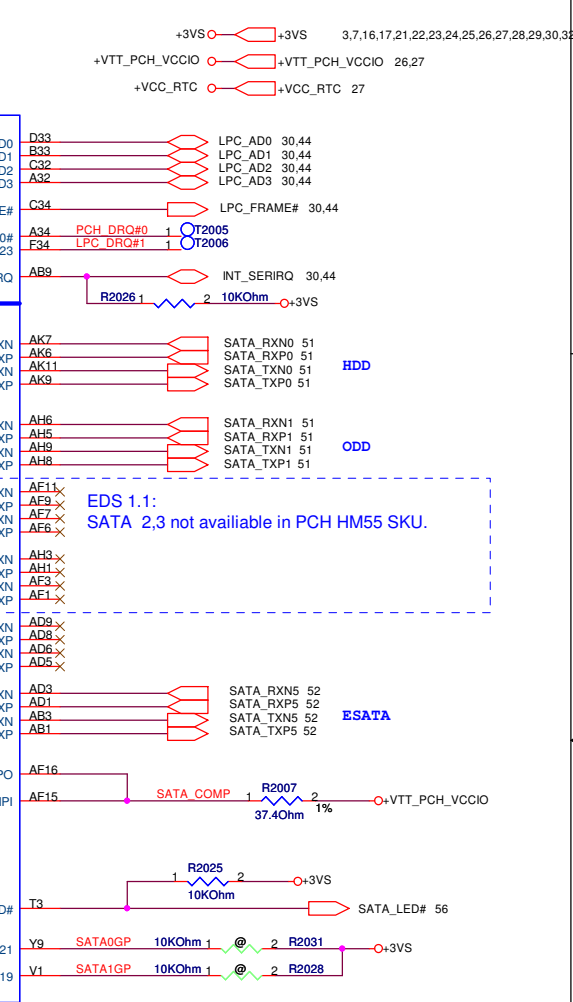
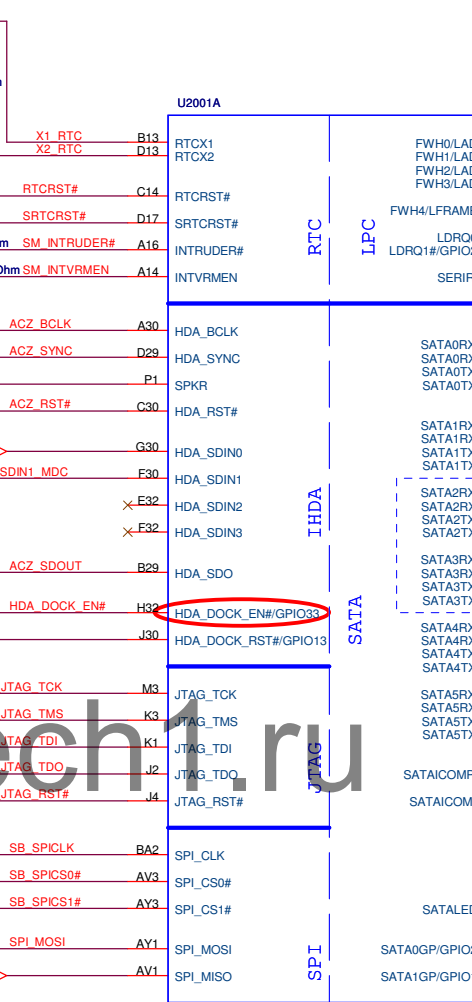
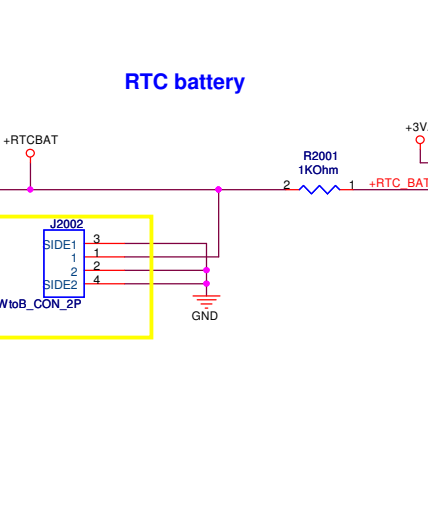
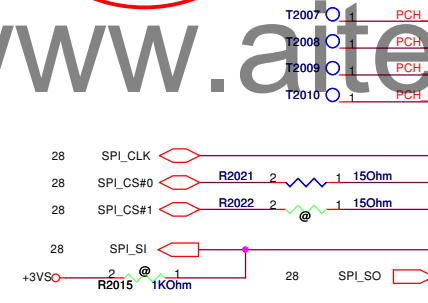
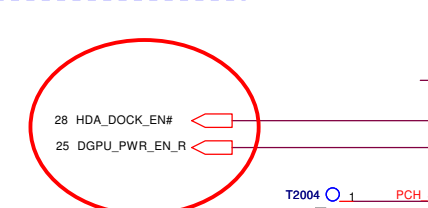
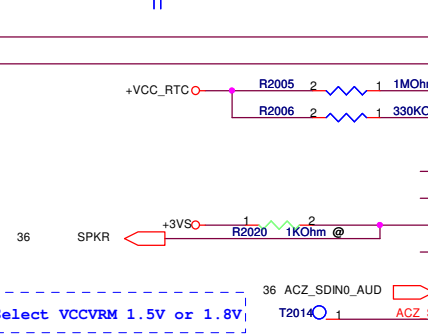
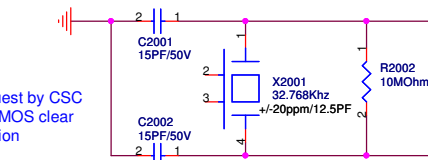
HDA_SPKR: No reboot strap
Low: Disable.
High: Enable

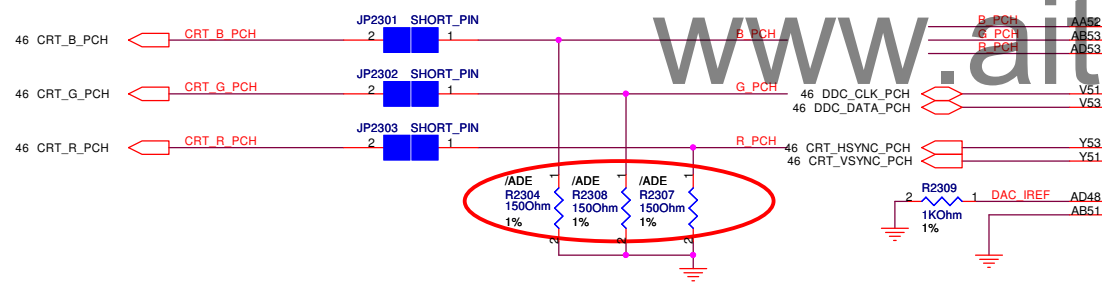
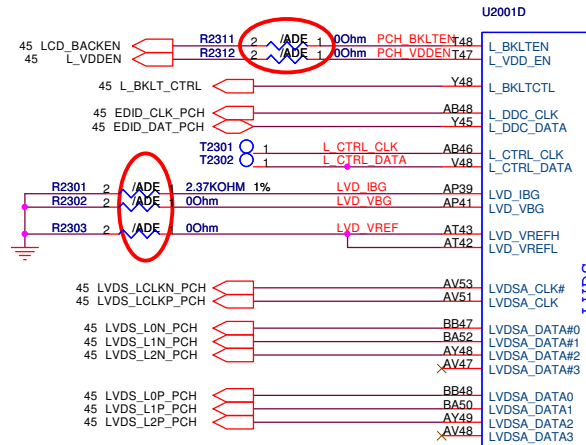
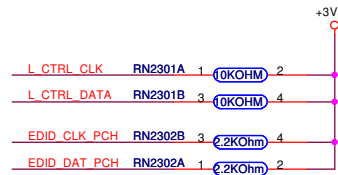
HDA_DOCK_EN#:
1. Flash descriptor security:
Sampled low: override
Sampled high: in effect.
2. GPIO33 low on the rising edge of PWROK,
Will also disable Intel ME.

SPI_MOSI: iTPM strap.
Mount R2015: Enable
Unmount R2015: Disable(default)



RTC battery

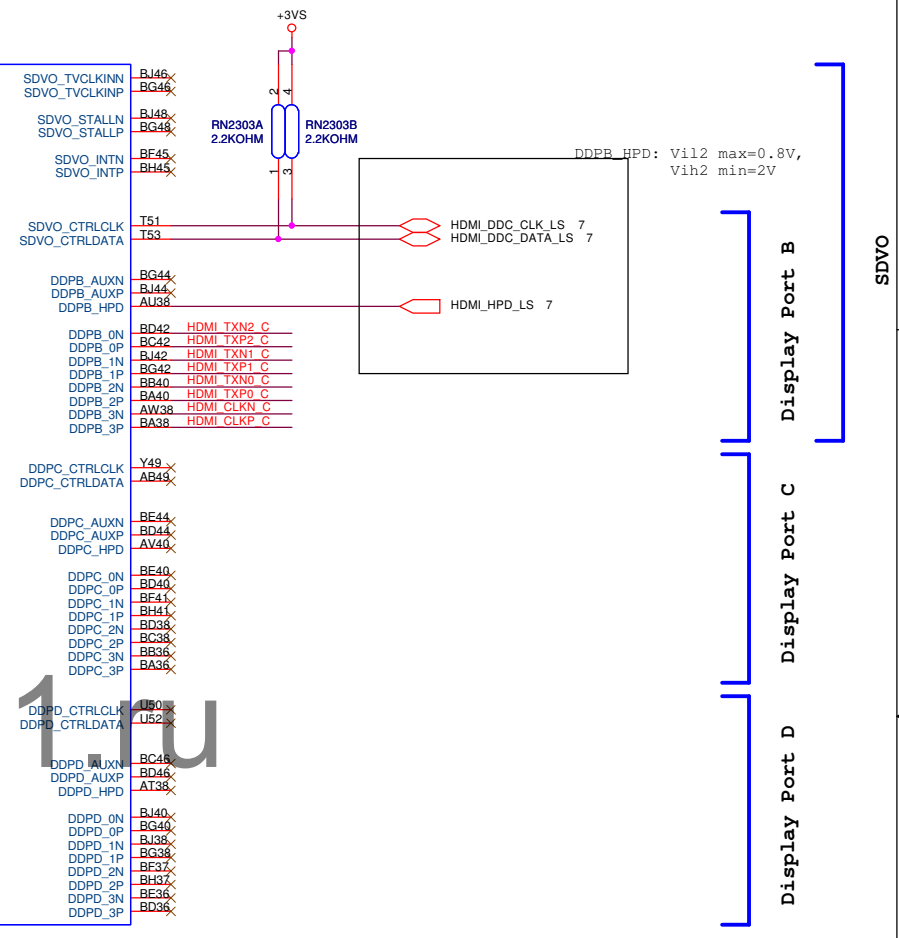




Digital Display Interface

CRT

BEXPEAK-M



Display Port Disable: (For discrete graphic)

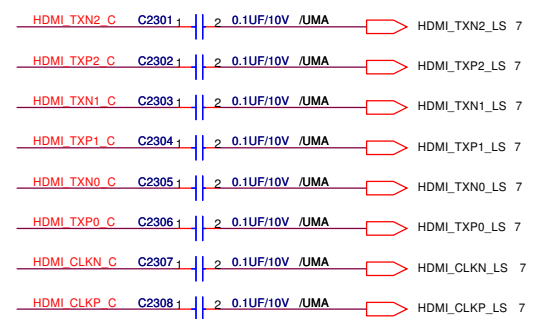
1. NC:
ALL

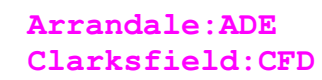
LVDS Disable: (For discrete graphic)

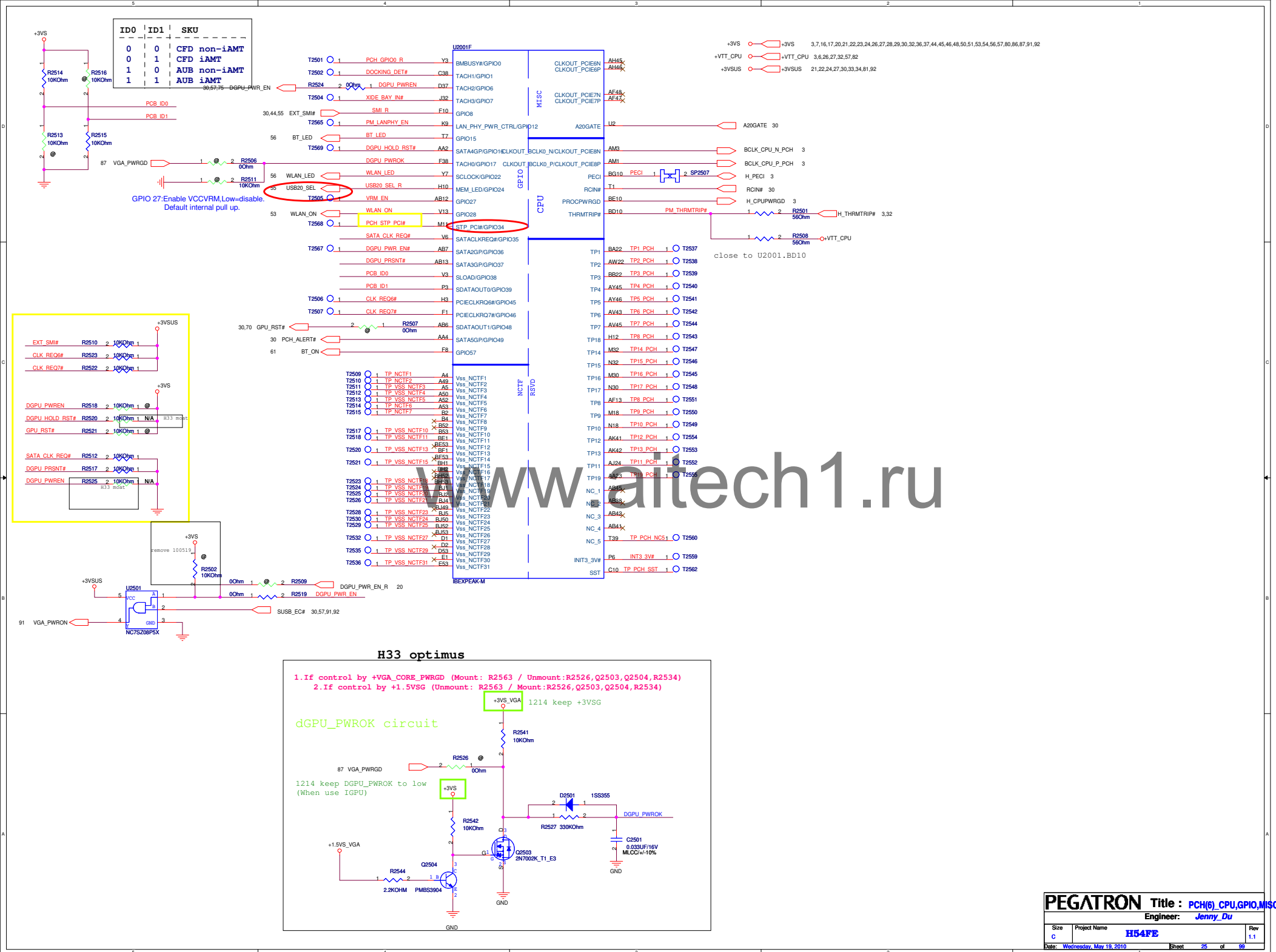
1. NC:
LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
VccALVDS, VccTX_LVDS

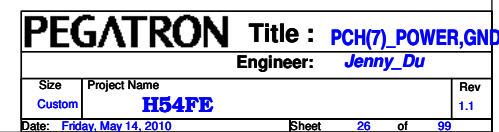
CRT Disable: (For discrete graphic)

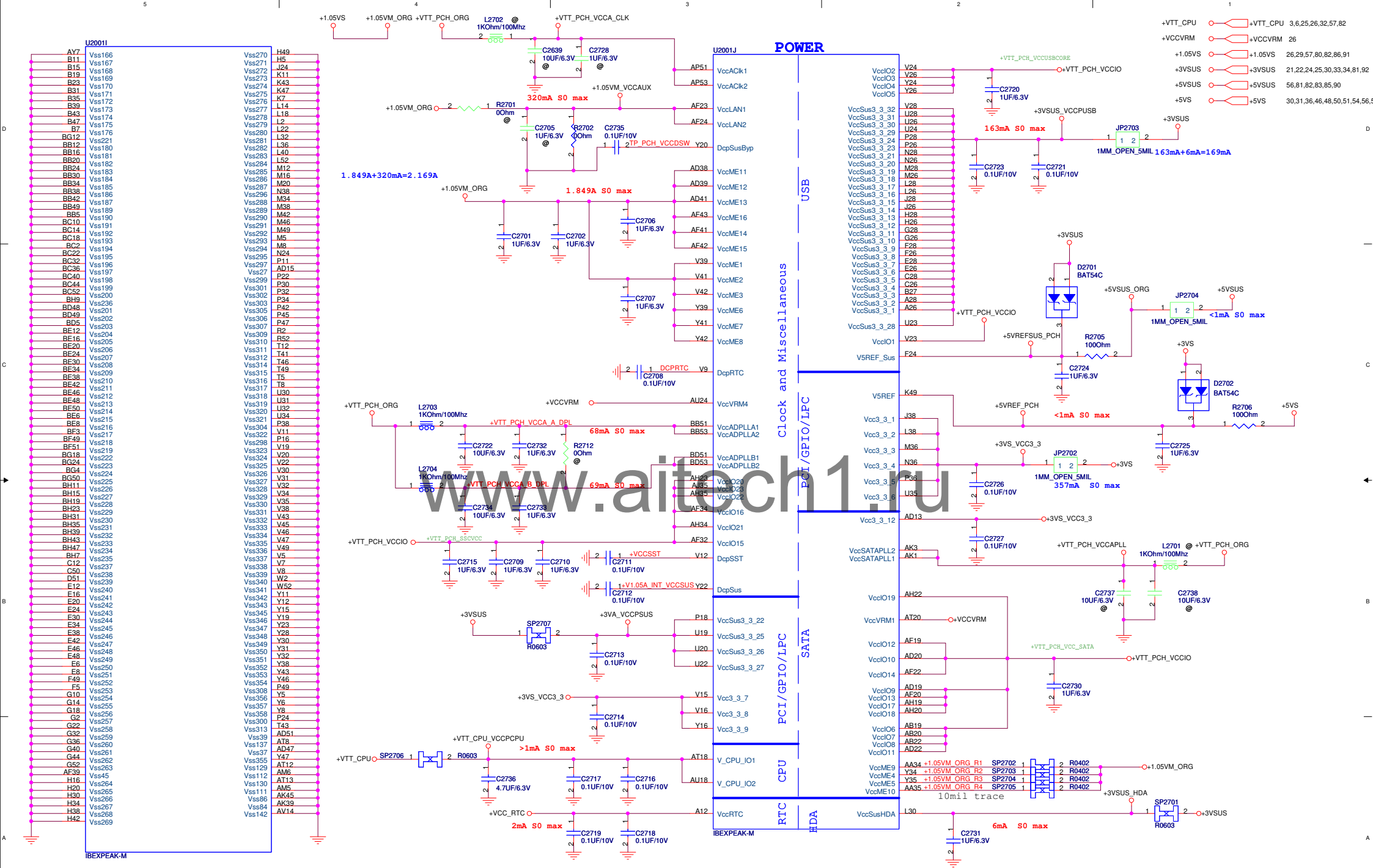
1. NC:
CRT_RED, CRT_GREEN, CRT_BLUE
CRT_HSYNC, CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
DAC_IREF
3. Connected to GND:
CRT_ITRN
4. Connect to +V3.3:
VCCADAC











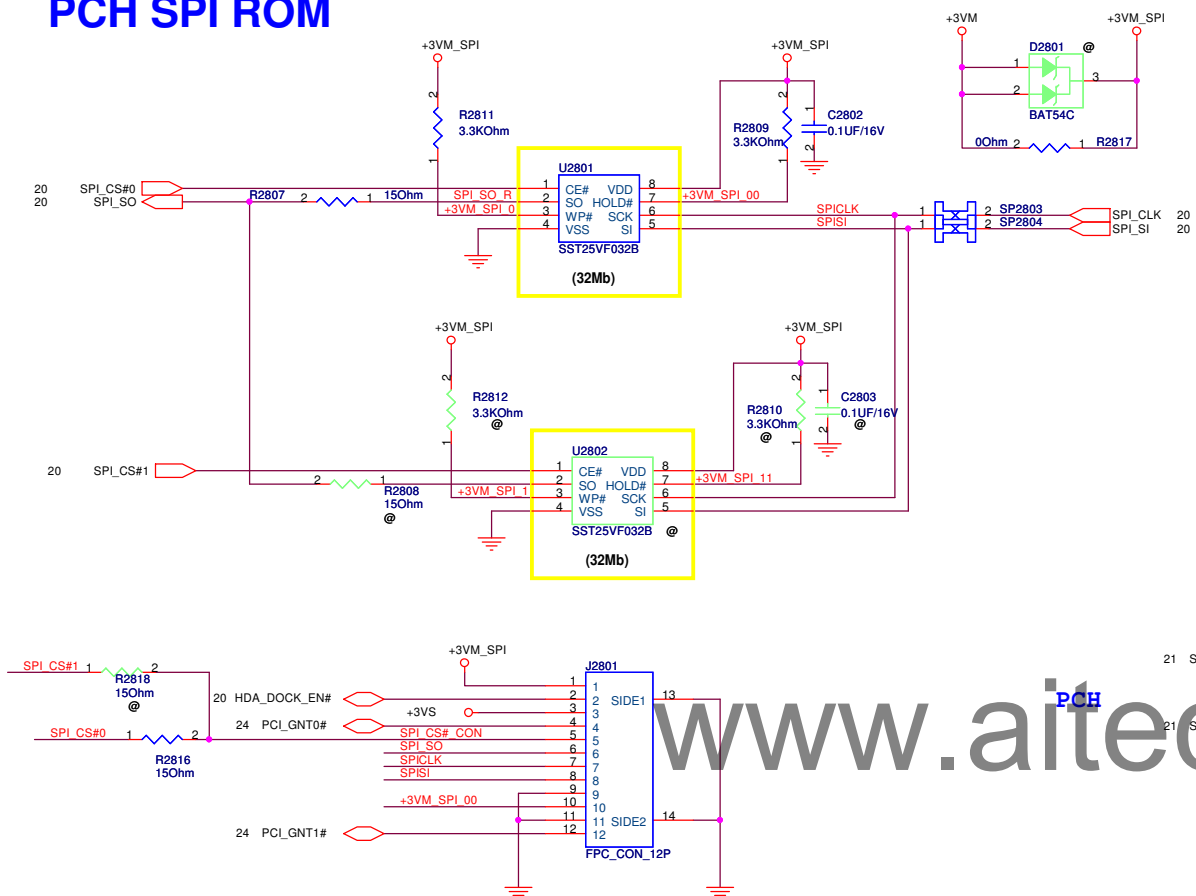
PEGATRON Title : PCH(8)_POWER,GND
Engineer: Jenny Du

Size	Project Name	Rev
Custom	H54FE	1.1

Date: Friday, May 14, 2010

Sheet 27 of 99

PCH SPI ROM

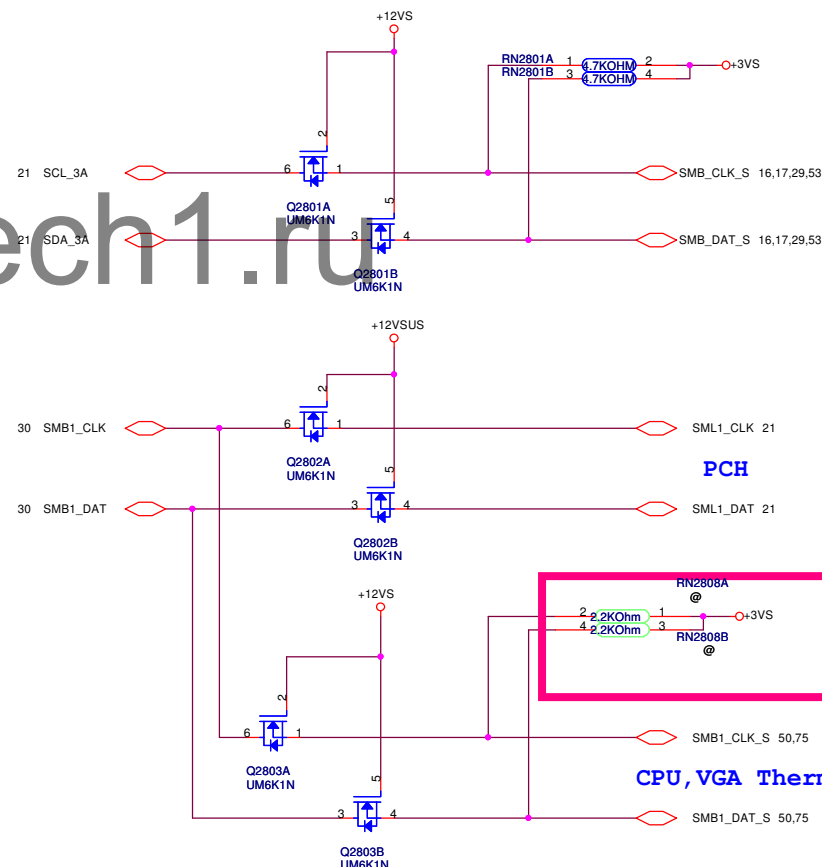
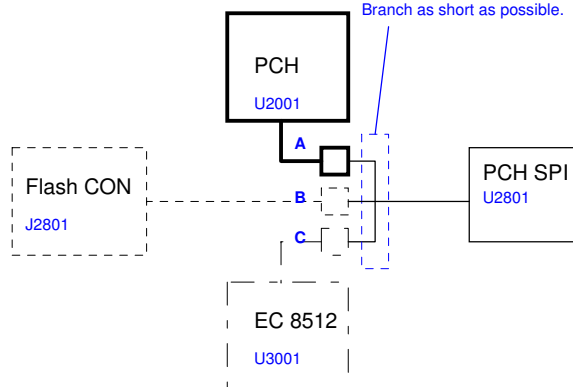


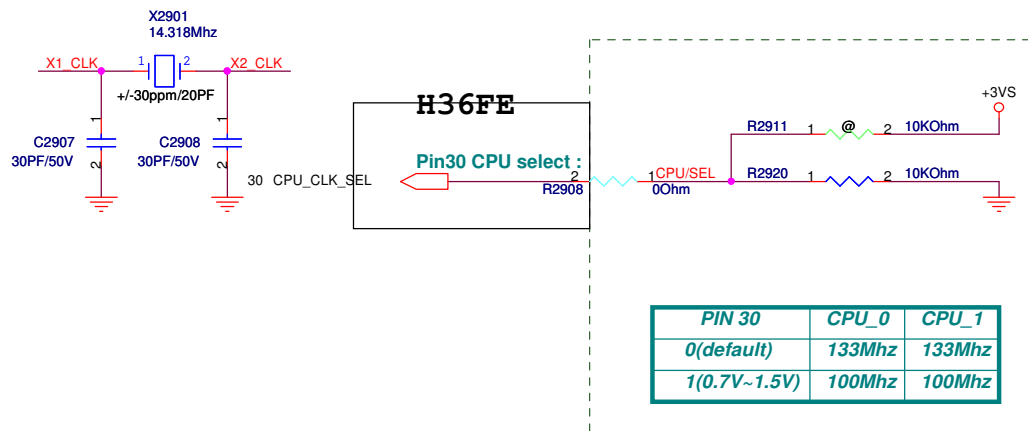
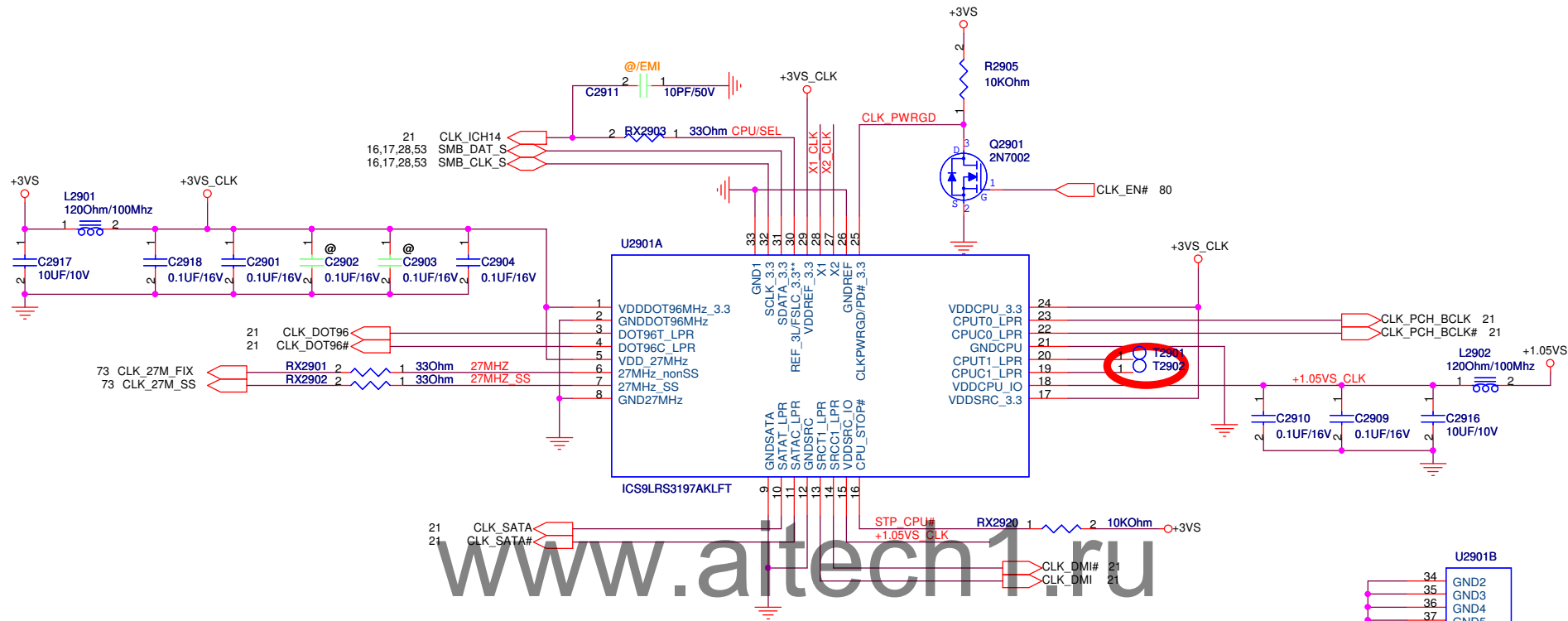
SMBUS Link device
DDR
CLKGEN
DEBUG
WLAN

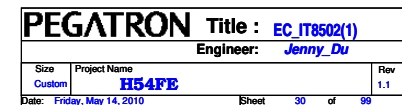
www.aitech1.ru

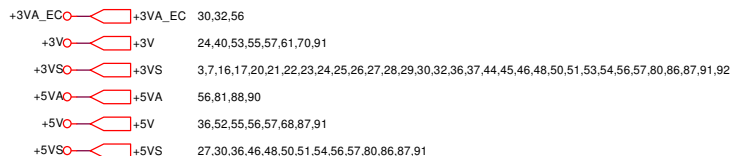
SPI Setting for layout:

Branch as short as possible.

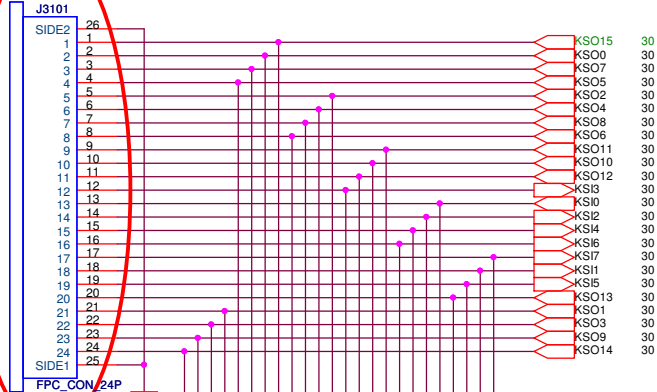




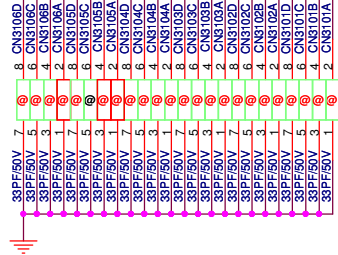




Keyboard V020462

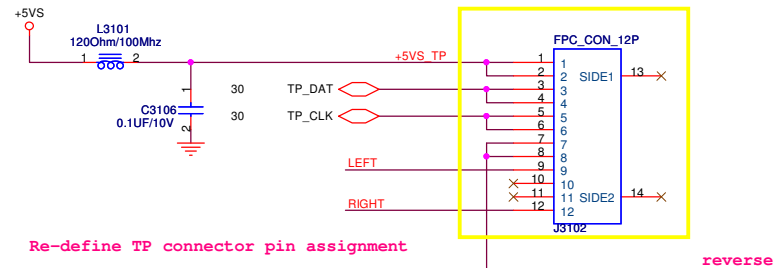


Reverse KB Connector.



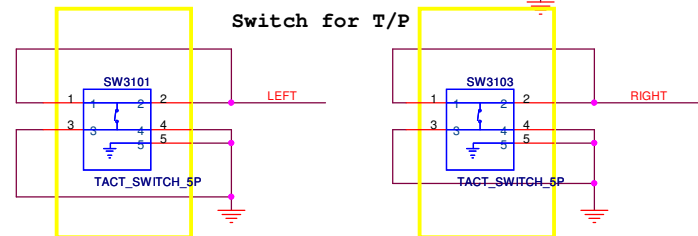
TOUCH PAD CONN

已换connector, 再check footprint



Re-define TP connector pin assignment

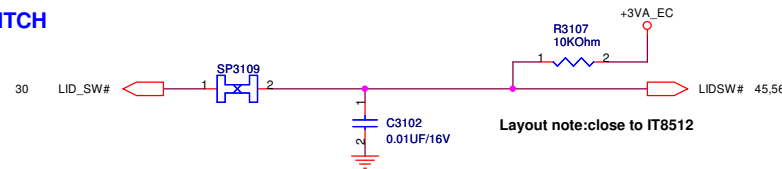
reverse



已更新 footprint

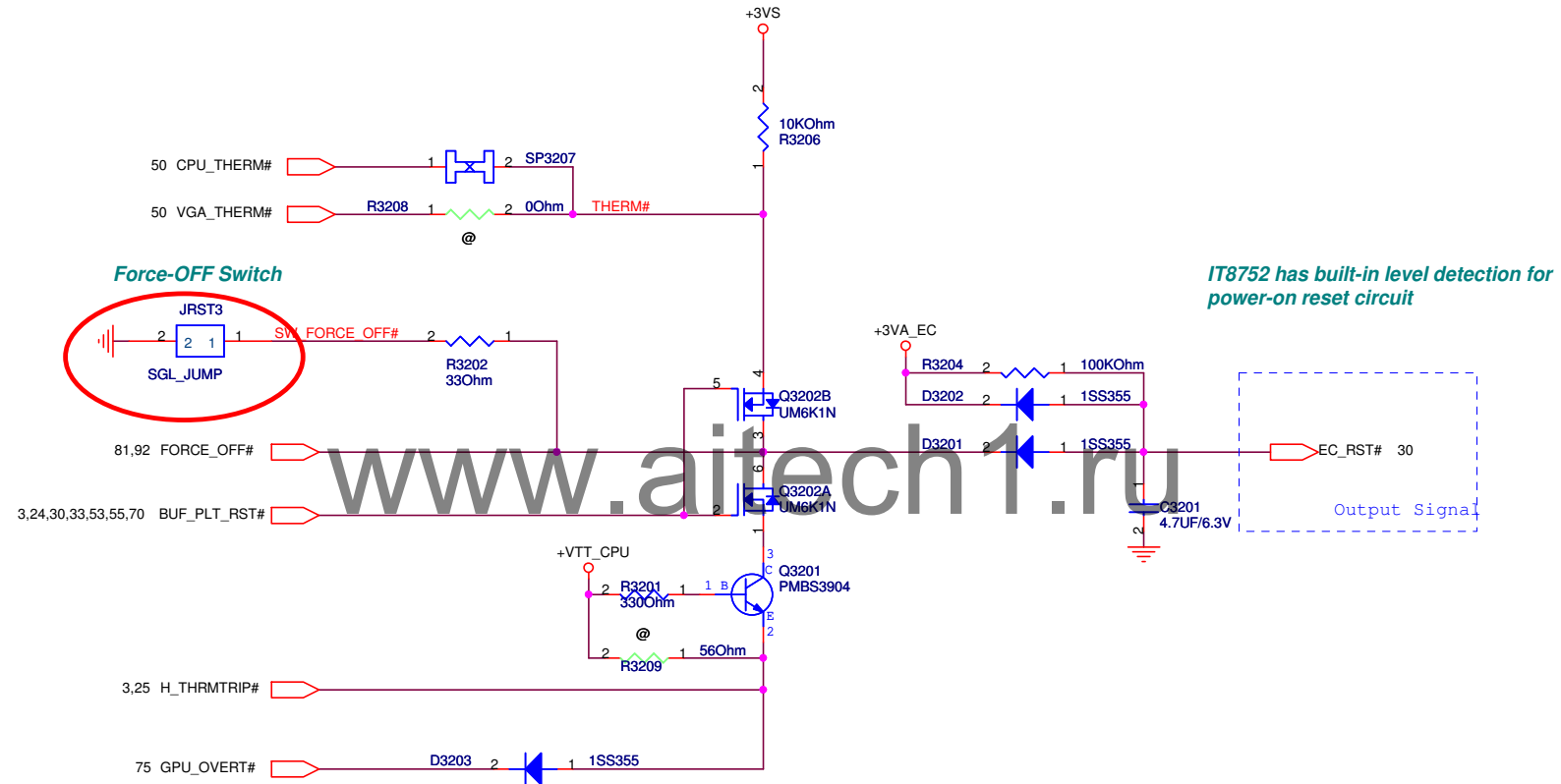
www.aitech1.ru

LID SWITCH

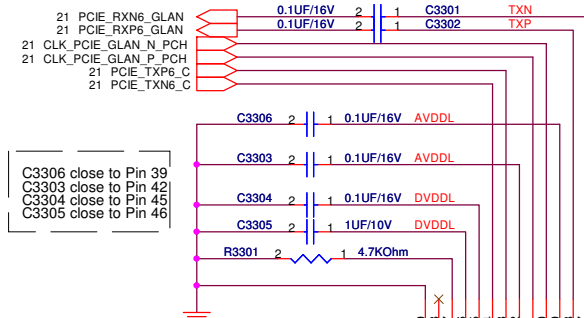


Layout note: close to IT8512

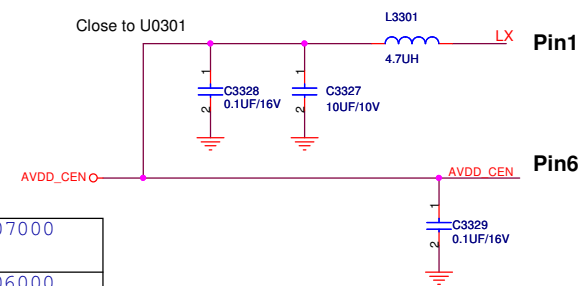
Thermal Policy



Power Table	PIN
3.3V Power	2
2.5V OUT	15
2.5V DVDDH	5
2.5V AVDDH	19,25
1.25V OUT	11
1.1V OUT	8
1.1V AVDDL	16,22,36,39,42
1.1V DVDD OUT	45,46
1.1V DVDDL	28,32
1.7V SWR	6
1.7V pin	1

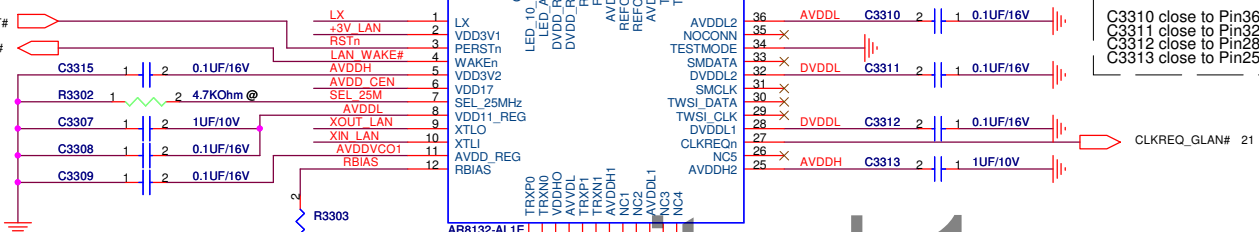


Giga	0200-0007000 AR8131
10/100	0200-0006000 AR8132

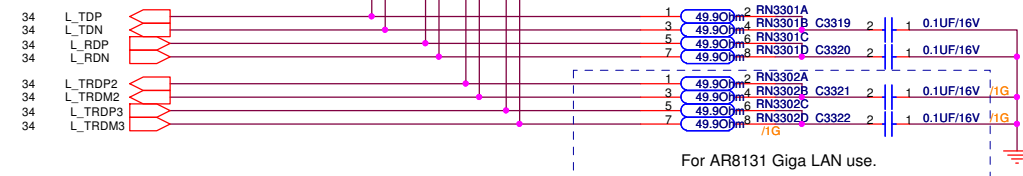


3,24,30,32,53,55,70 BUF_PLT_RST#
22,53 PCIE_WAKE#

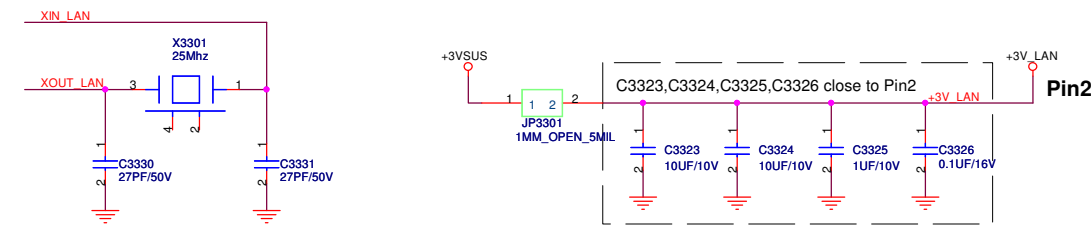
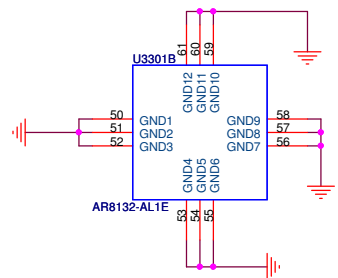
C3315 close to Pin 5
C3307 close to Pin 8
C3308 close to Pin 9
C3309 close to Pin 11

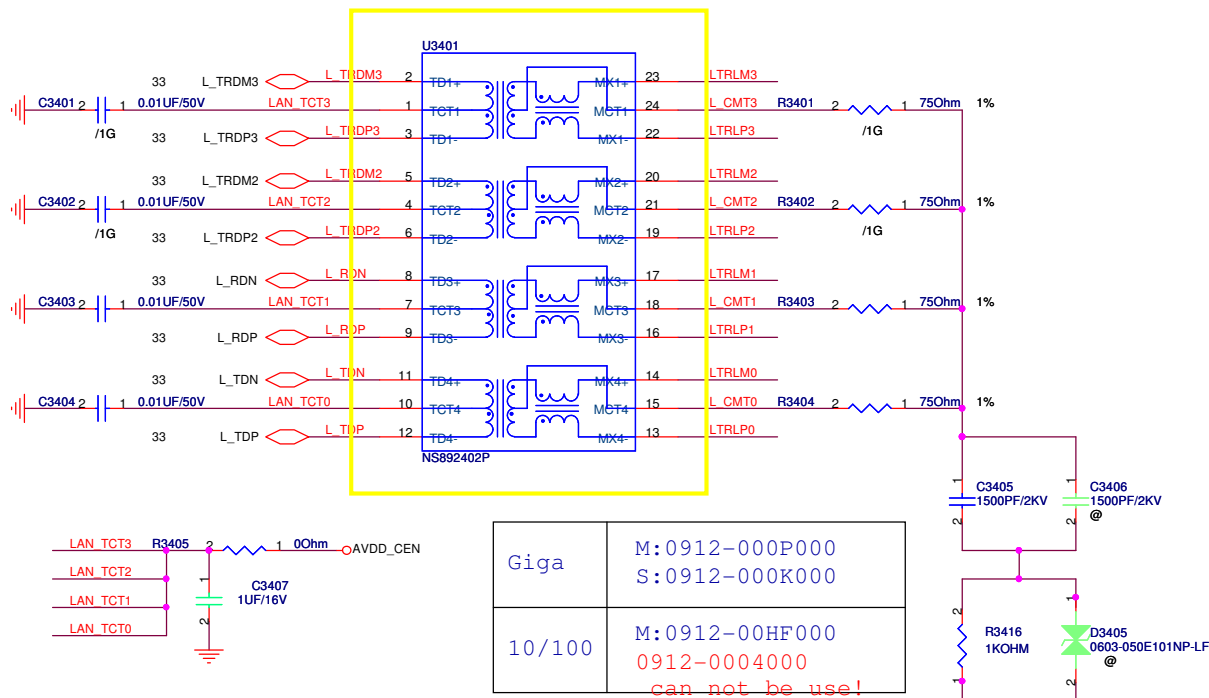


C3314 close to Pin22
C3316 close to Pin19
C3317 close to Pin16
C3318 close to Pin15

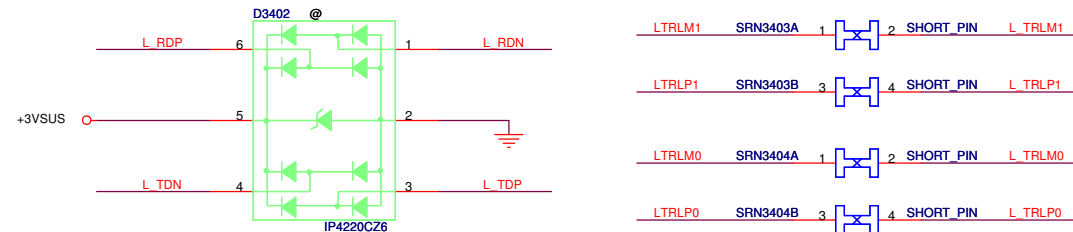
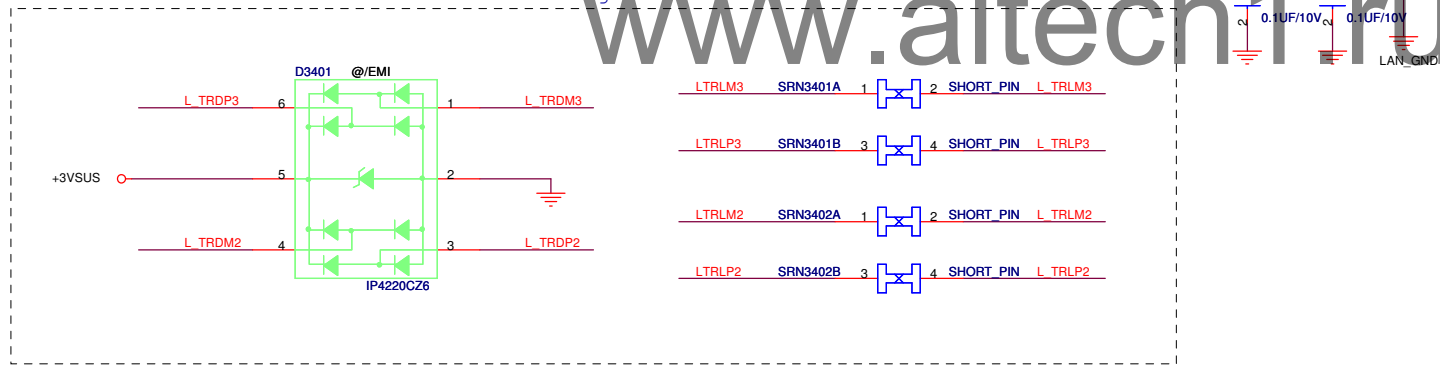


Termination Resistor Place near LAN chip



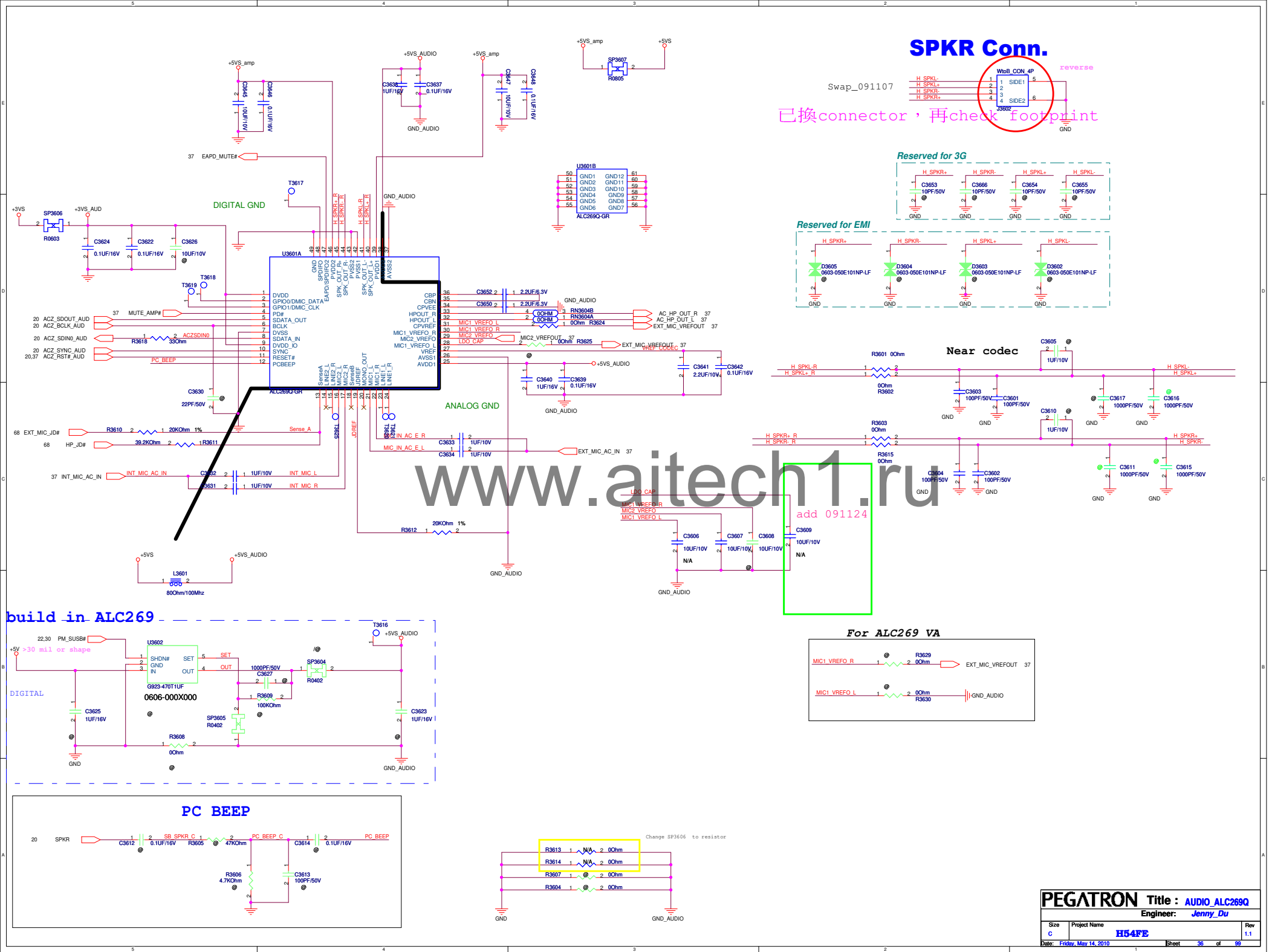


For AR8131 Giga LAN use.

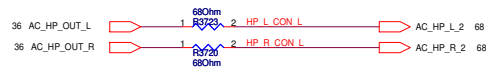


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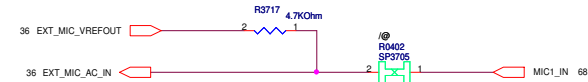
PEGATRON		Title :	
		Engineer: <i>Jenny_Du</i>	
Size A	Project Name H54FE		Rev 1.1
Date: <i>Friday, May 14, 2010</i>		Sheet	35 of 99



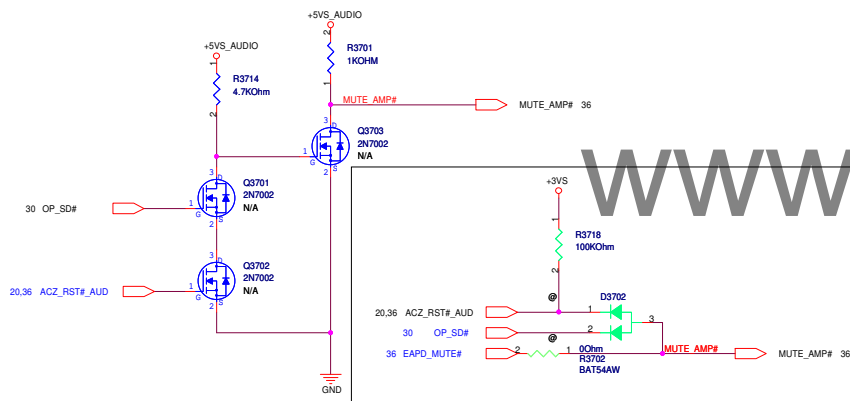
Headphone Jack



External Microphones

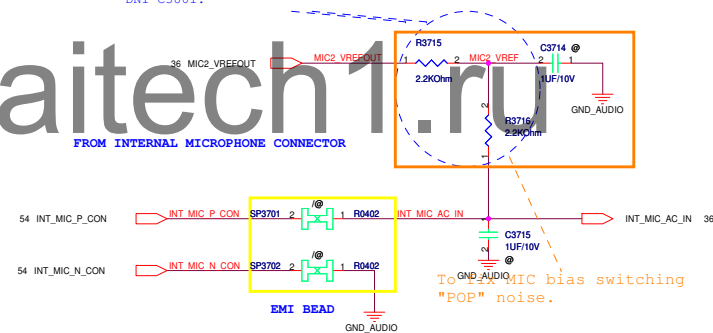


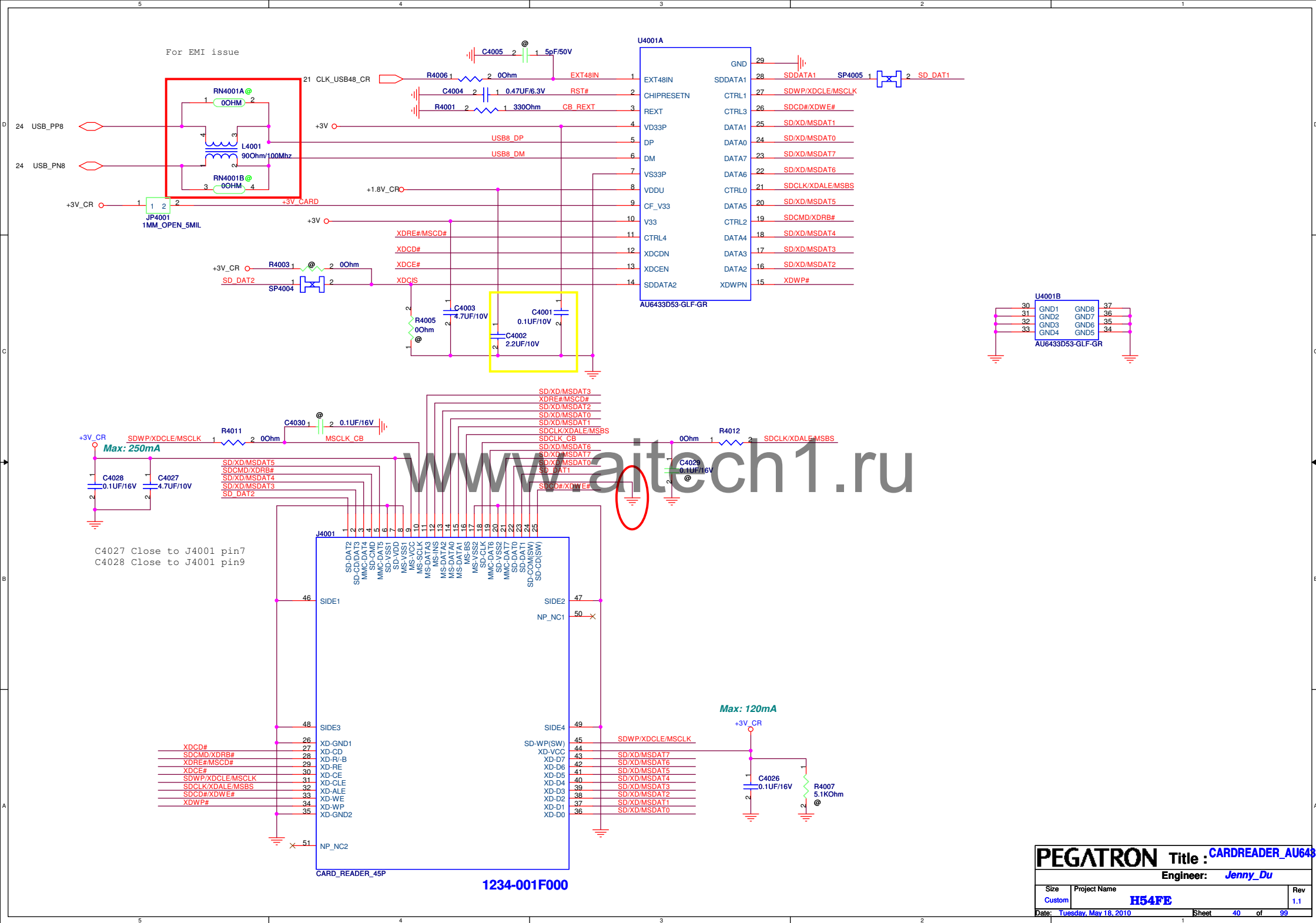
Mute Circuit



INTERNAL MICROPHONE

If EAPD available(fix MIC bias switching
"POP" noise):
Replace R3801,R3802 by one 4.7K ohm resistor.
DNI C3801.

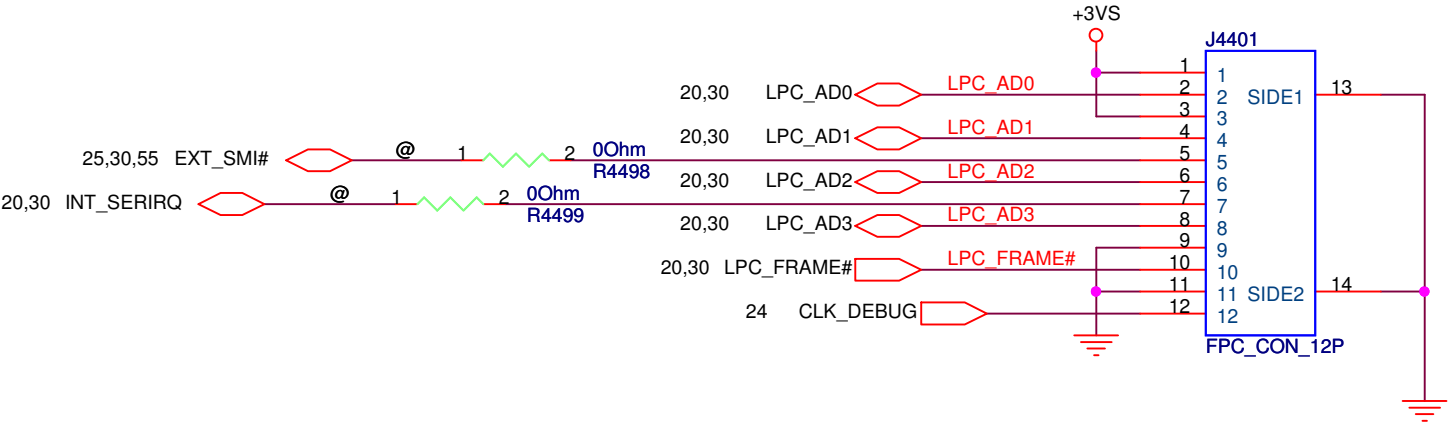




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PEGATRON		Title : CB(4)_NEWCARD	
BG1/RD3		Engineer: Jenny_Du	
Size B	Project Name H54FE		Rev 1.1
Date: Friday, May 14, 2010		Sheet 43 of 99	

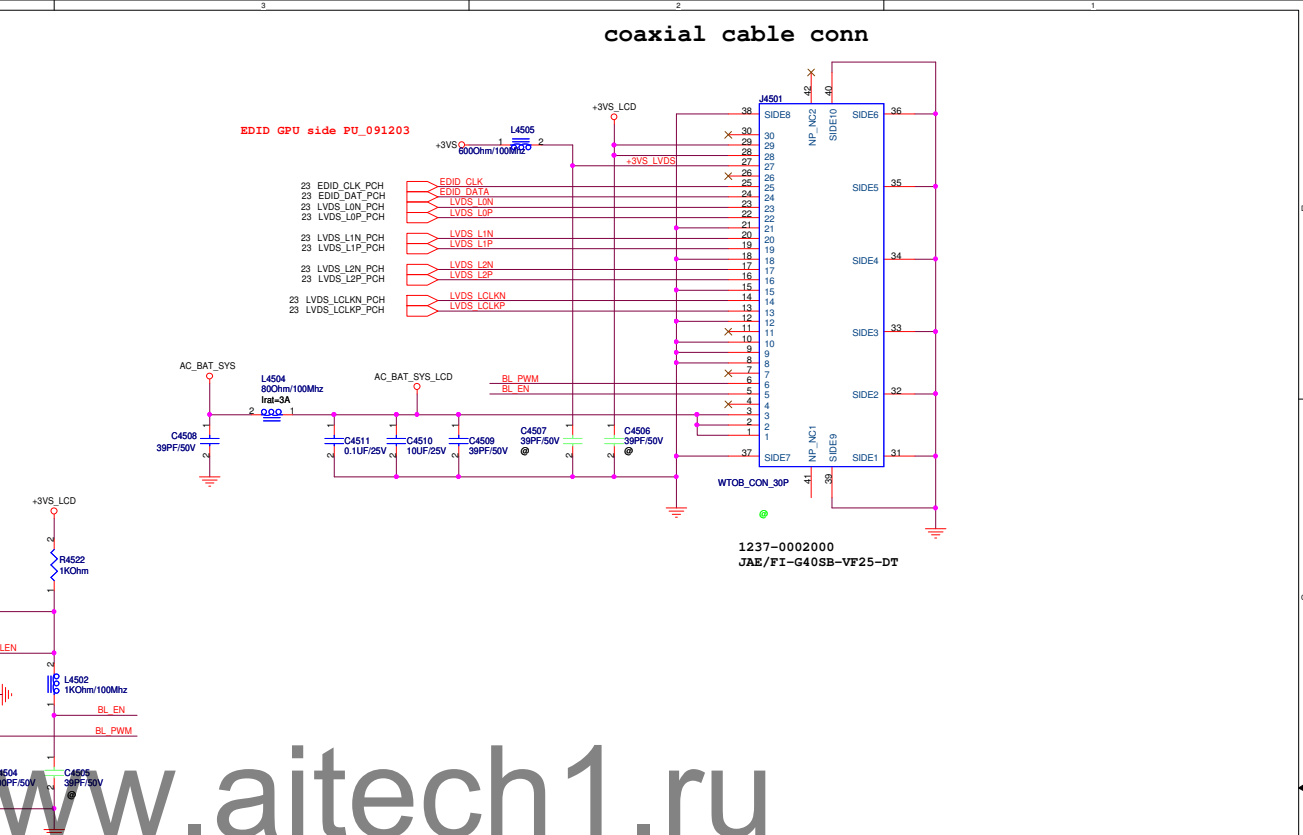
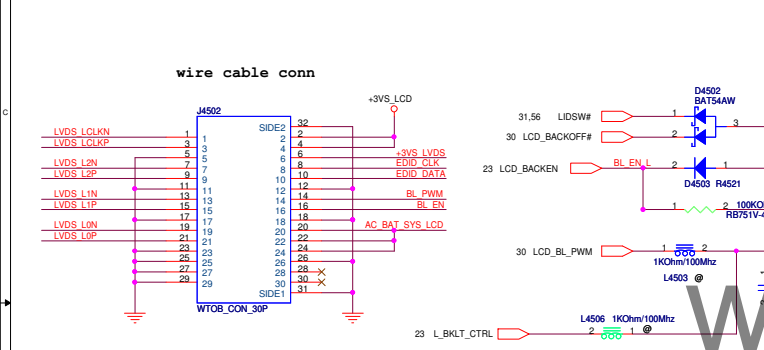
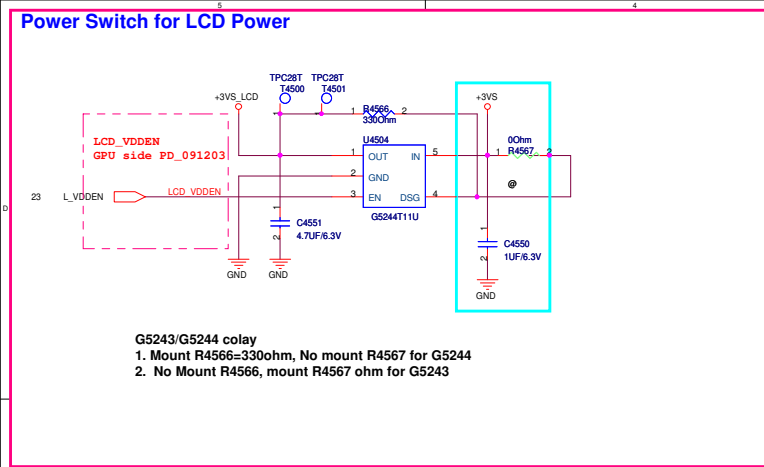
LPC Debug Port



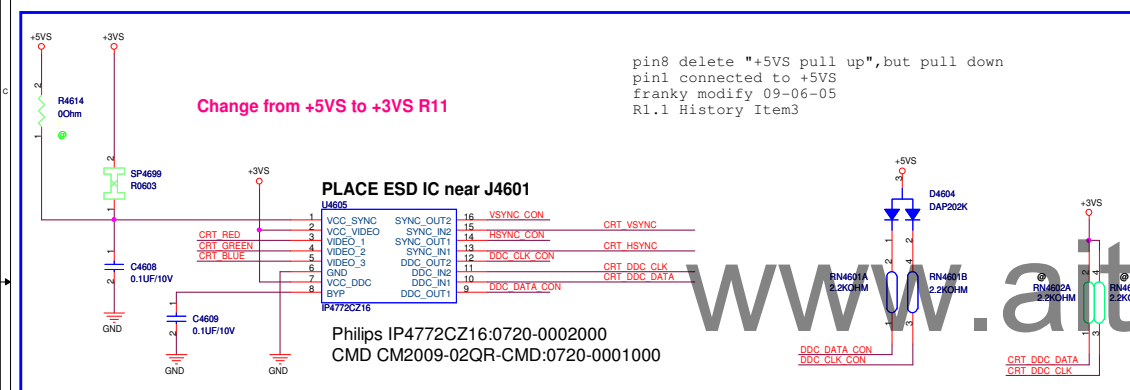
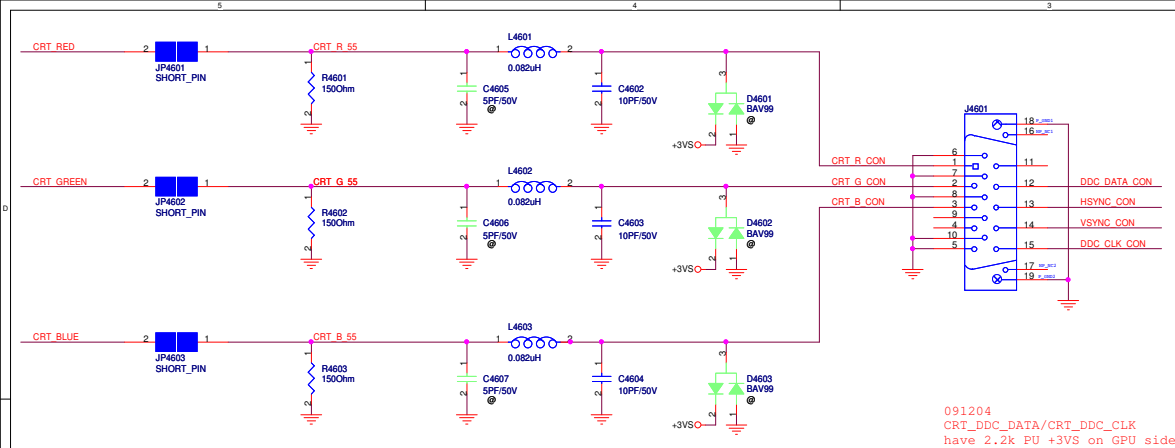
www.aitech1.ru

+3VS 3,7,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,45,46,48,50,51,53,54,56,57,80,86,87,91,92

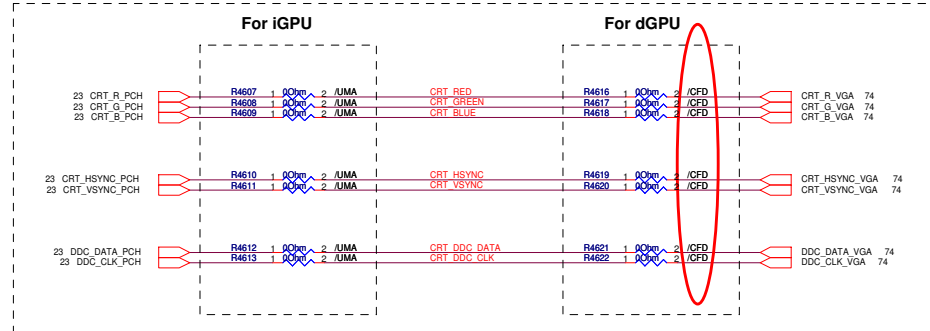
PEGATRON		Title : BUG_Debug	
BG1/RD3		Engineer: Jenny_Du	
Size A	Project Name H54FE		Rev 1.1
Date: Friday, May 14, 2010		Sheet 44	of 99



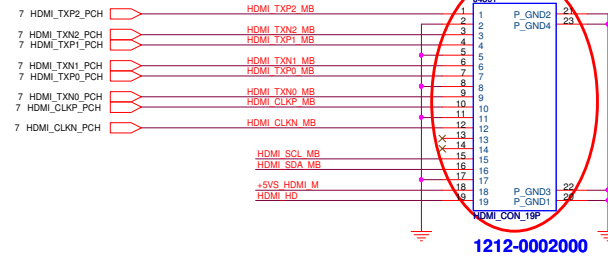
www.aitech1.ru



For non-Switchable Gfx



For Nvidia

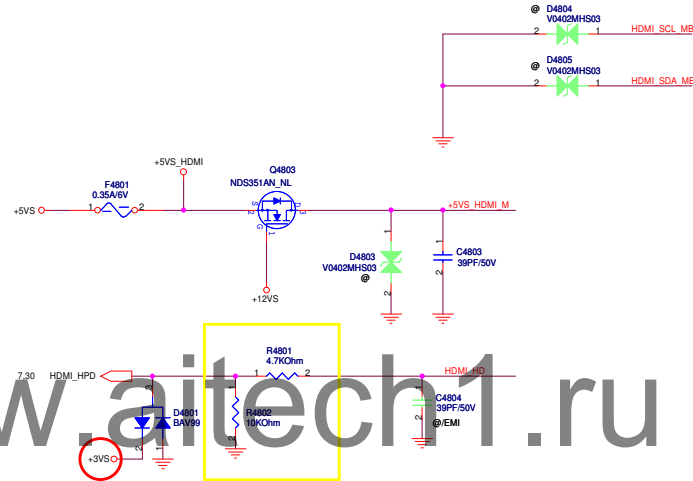
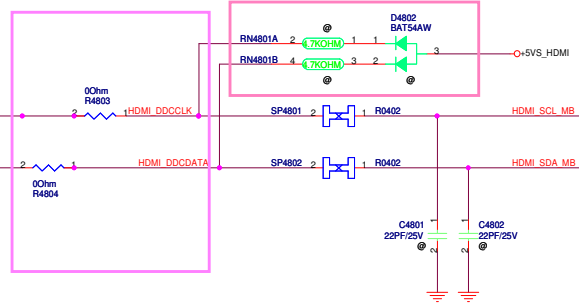


已換connector，再check footprint

Follow G60Jx_GPU have 2.2k PU +3VS_VGA

For UMA

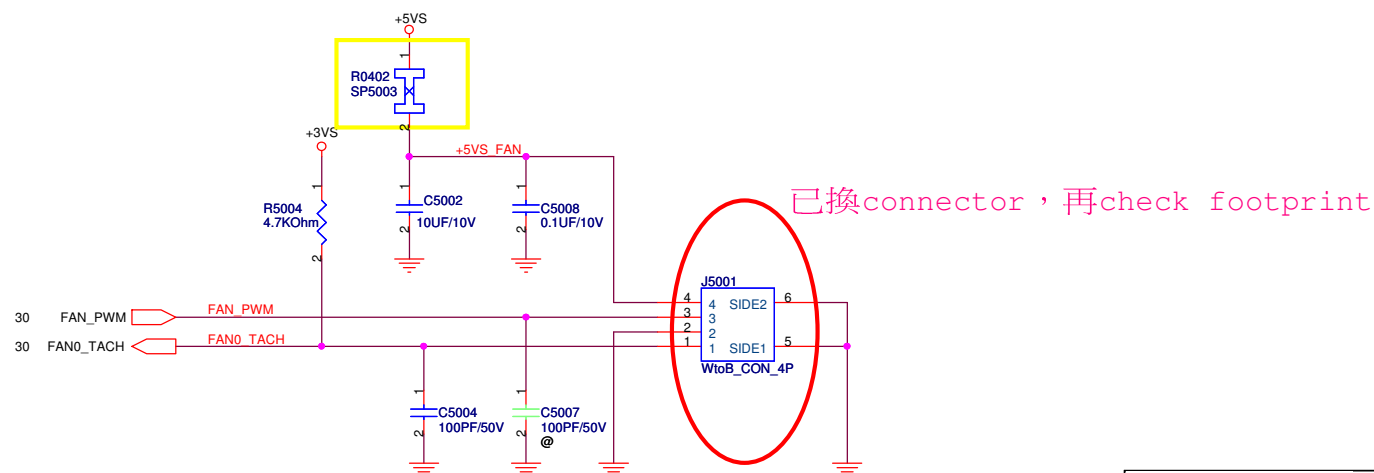
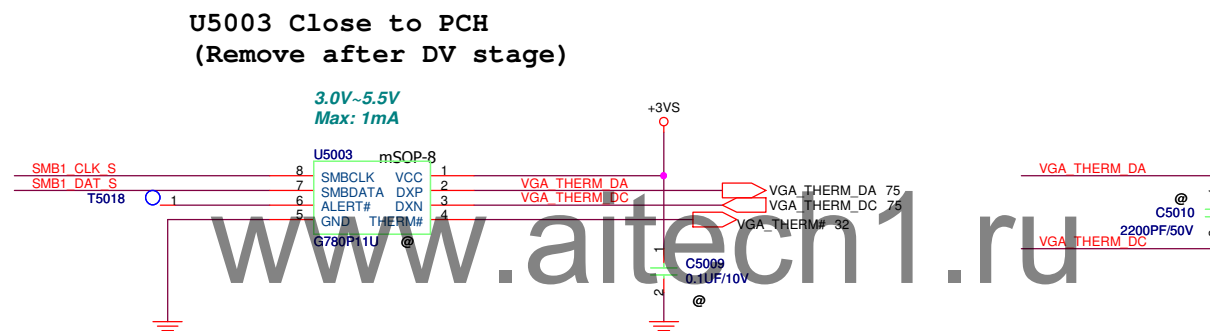
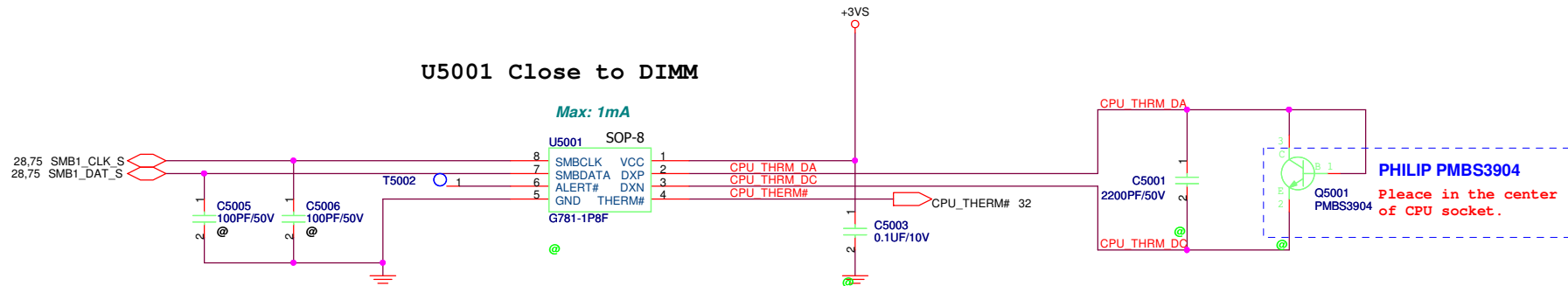
check again!



之後check discrete 是否可刪除

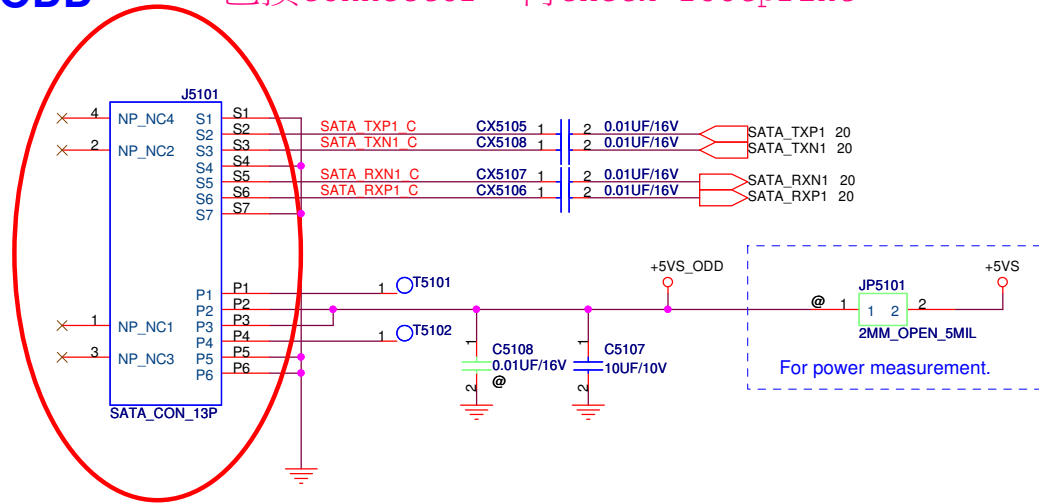
www.aitech1.ru

PEGATRON		Title : BOM OPTION	
Engineer: Jenny_Du			
Size A	Project Name H54FE		Rev 1.1
Date: Friday, May 14, 2010		Sheet	49 of 99



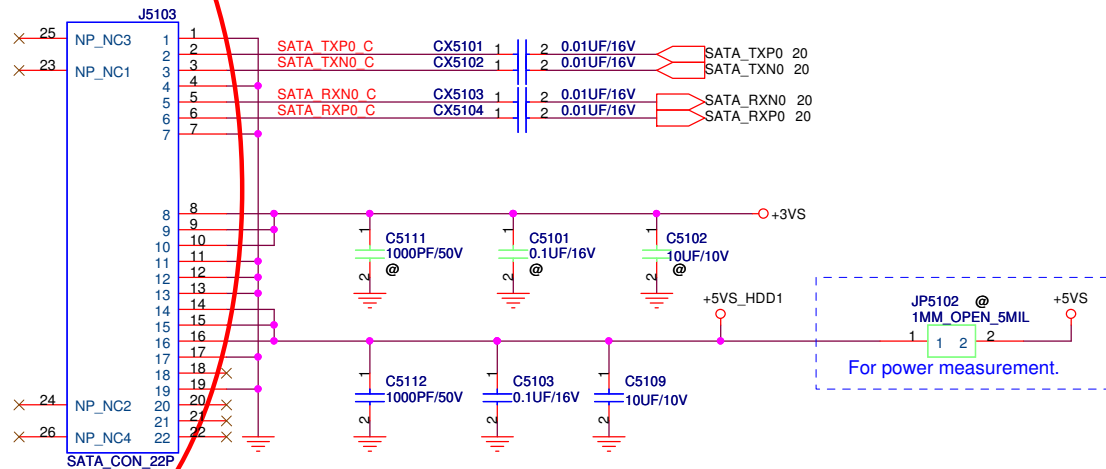
ODD

已換connector，再check footprint



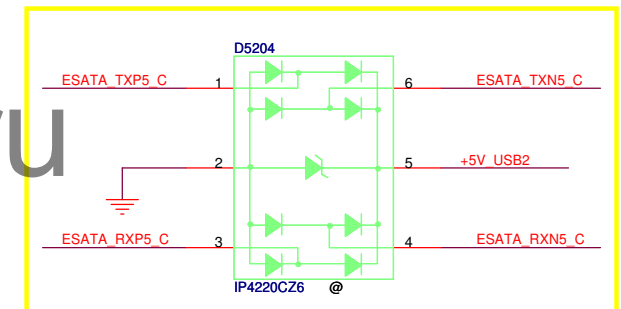
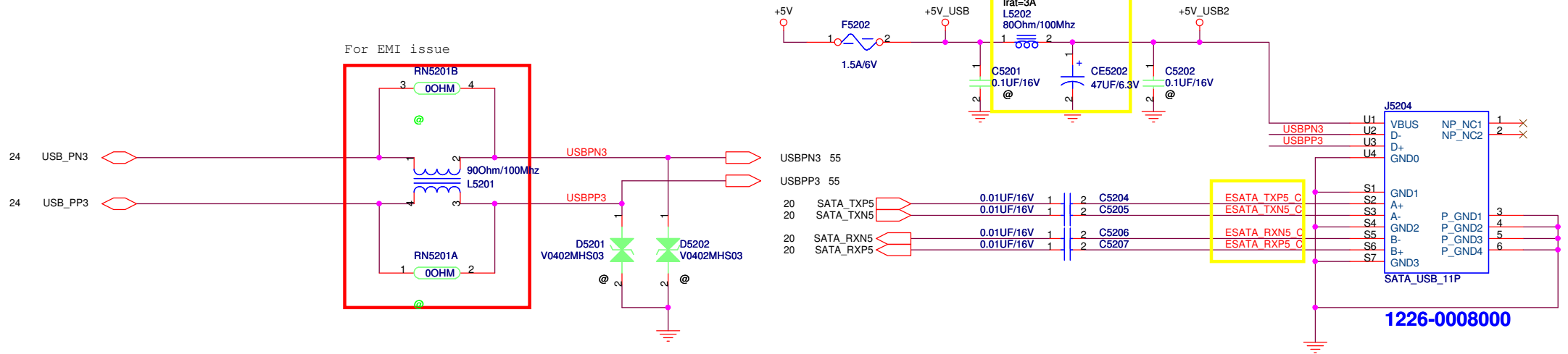
HDD

已換connector，再check footprint




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已換connector， footprint需在check

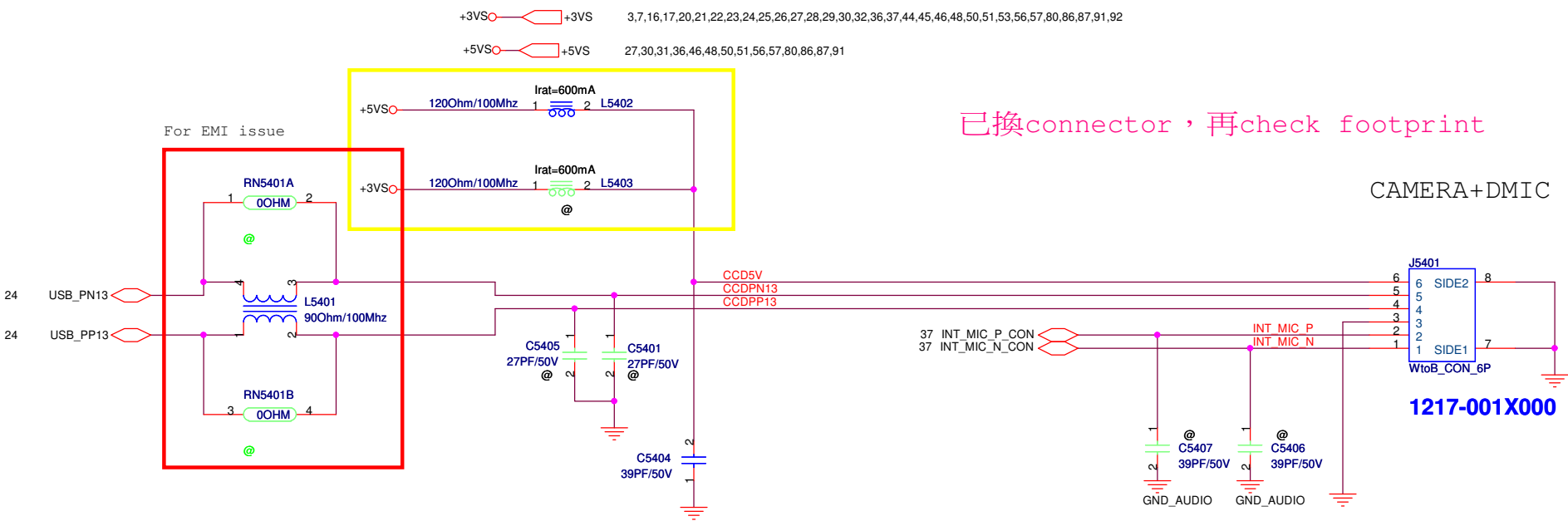


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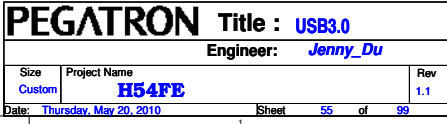
 H5302
CT217B67D47
1308-0008000

PEGATRON		Title : <i>WLAN / WWAN</i>	
		Engineer: <i>Jenny_Du</i>	
Size B	Project Name H54FE	Rev 1.1	
Date: <i>Friday, May 14, 2010</i>		Sheet <i>53</i>	of <i>99</i>

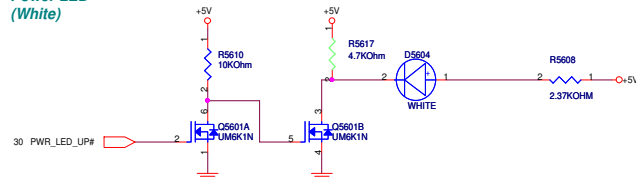


已換connector，再check footprint

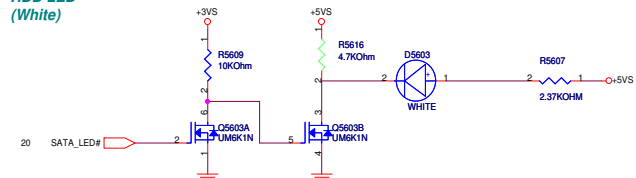
www.aitech1.ru



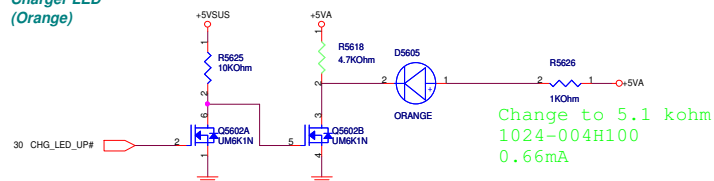
Power LED (White)



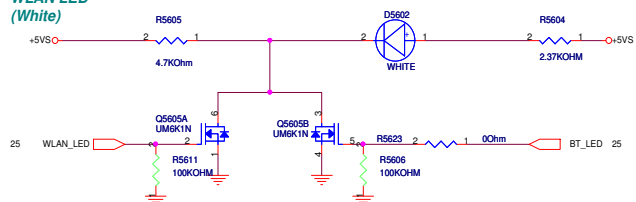
HDD LED (White)



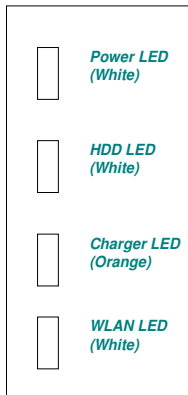
Charger LED (Orange)



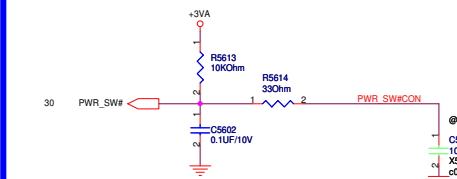
WLAN LED (White)



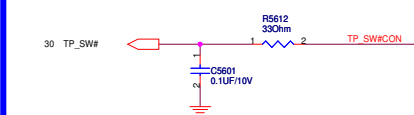
LED Placement



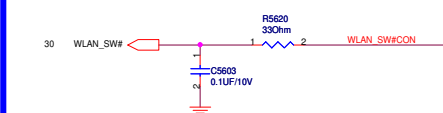
Power Button



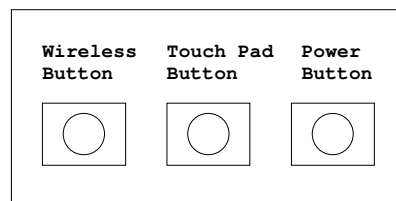
Touch Pad Button



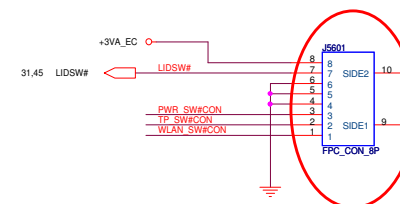
Wireless Button

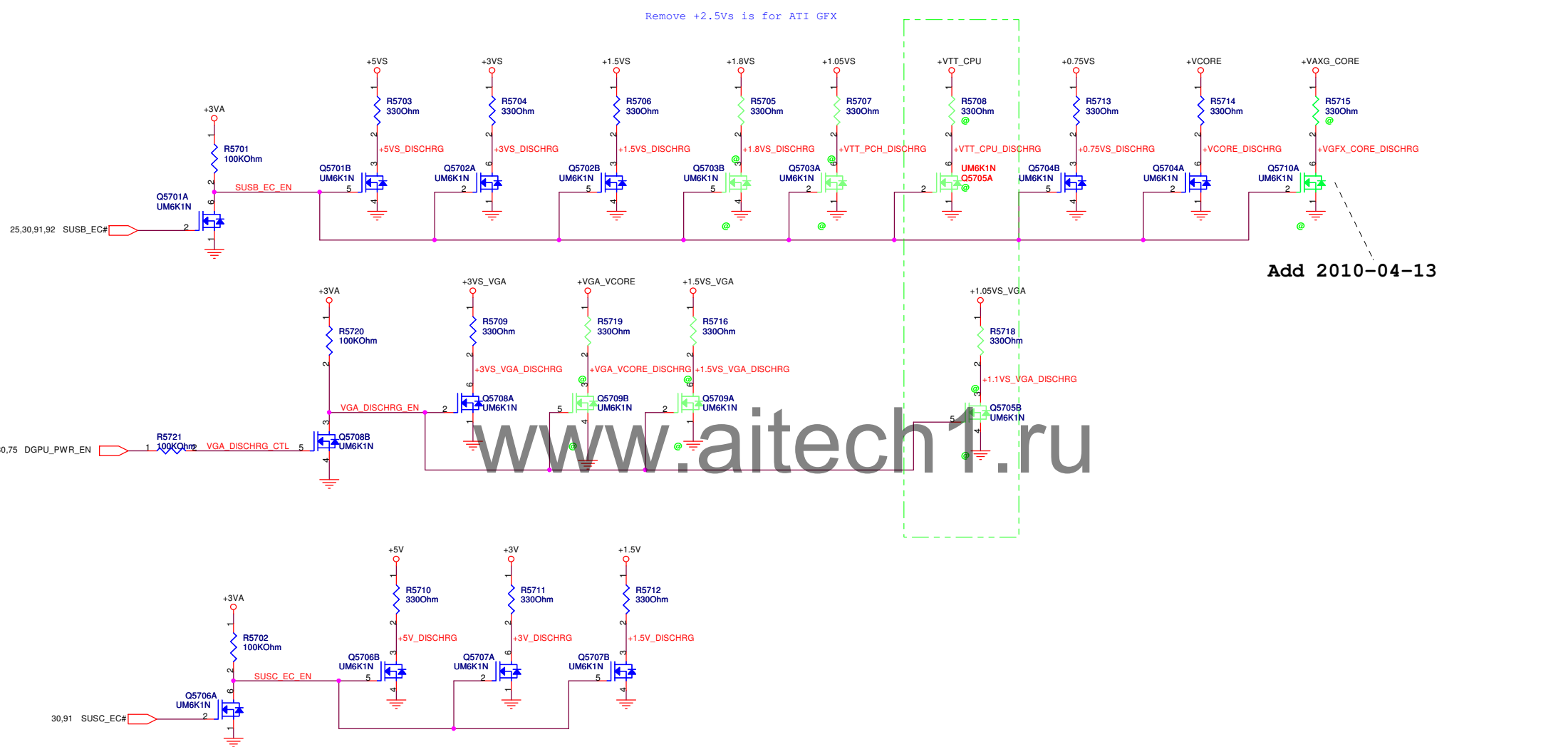


Switch Board Placement

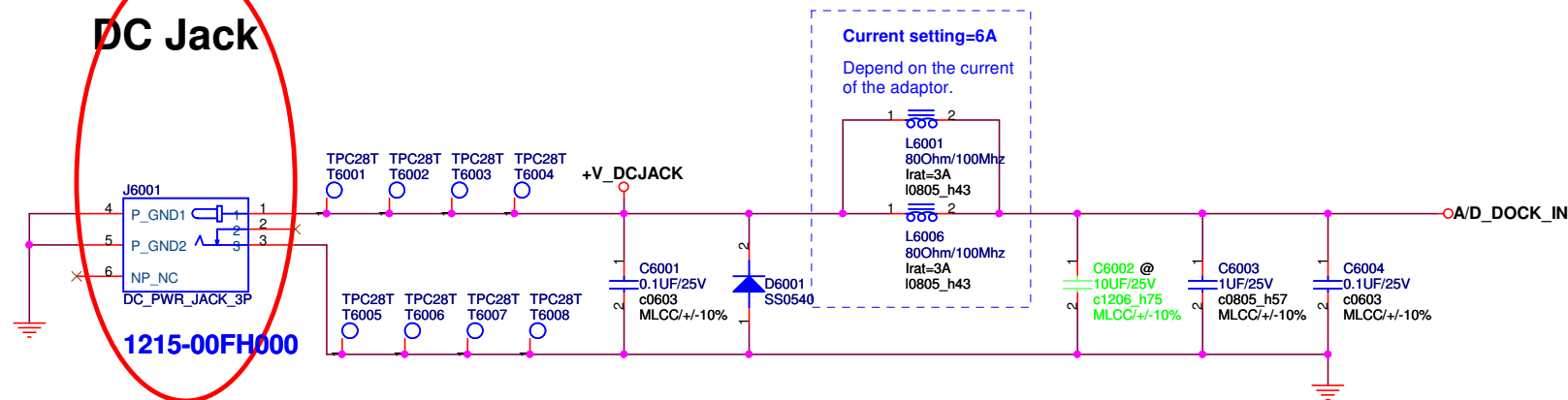


Function BD



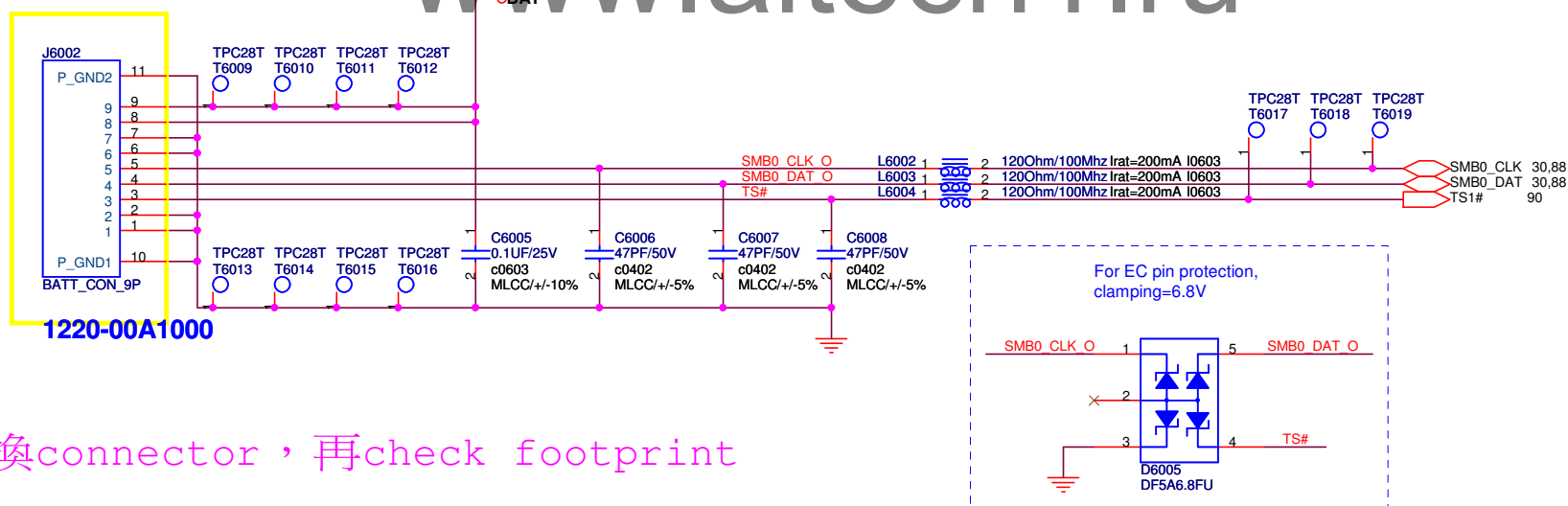


DC Jack

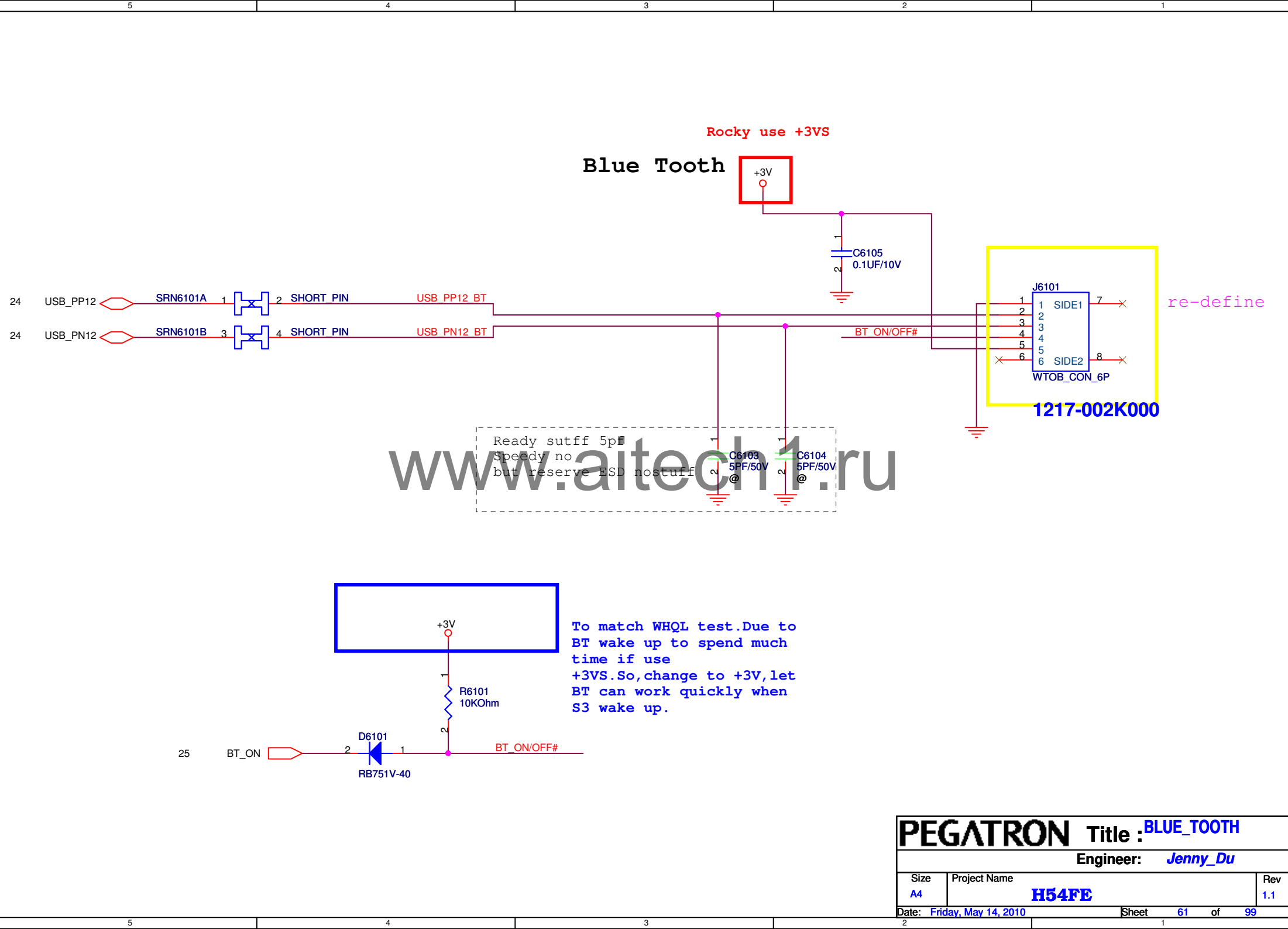


已換connector，需再check footprint。

Battery Connector



已換connector，再check footprint



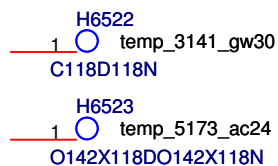
www.aitech1.ru

PEGATRON		Title :	
BG1/RD3		Engineer: Jenny_Du	
Size A	Project Name H54FE		Rev 1.1
Date: Friday, May 14, 2010		Sheet	62 of 99

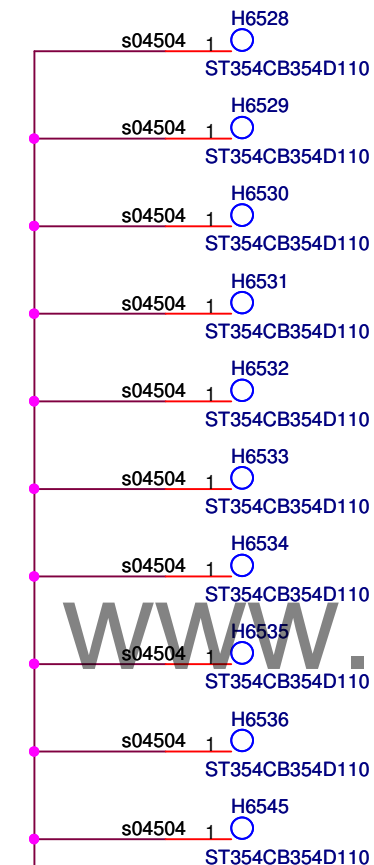
www.aitech1.ru

PEGATRON		Title : FINGER PRINT	
Engineer: Jenny_Du			
Size A	Project Name H54FE		Rev 1.1
Date: Friday, May 14, 2010		Sheet 63	of 99

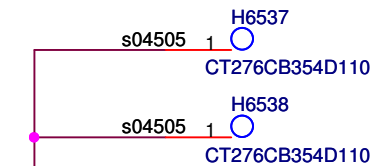
Tooling hole x 2



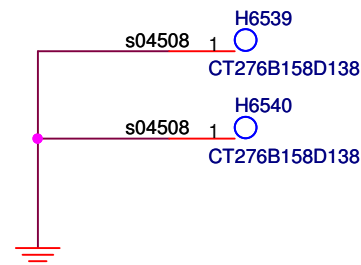
"A" FOR configuration x 9



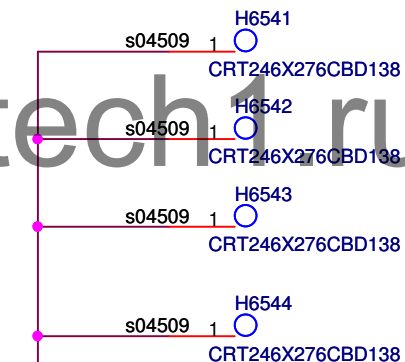
"B" FOR configuration x 2



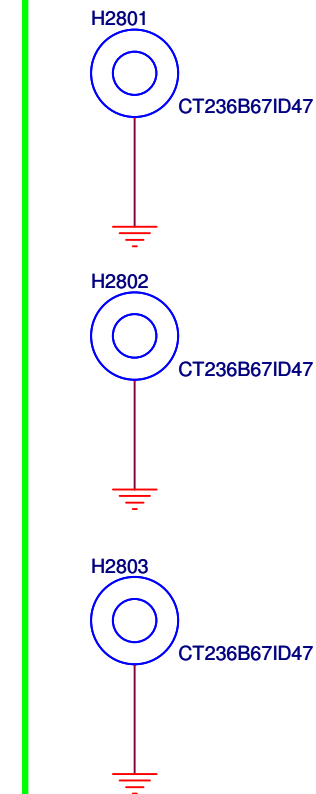
"C" FOR GPU x 2



"D" FOR CPU x 4



H36T PCH Sink



PEGATRON		Title : ME_CONN,Skew Hole	
		Engineer: Jenny_Du	
Size A	Project Name H54FE		Rev 1.1
Date: Friday, May 14, 2010		Sheet 65 of 99	

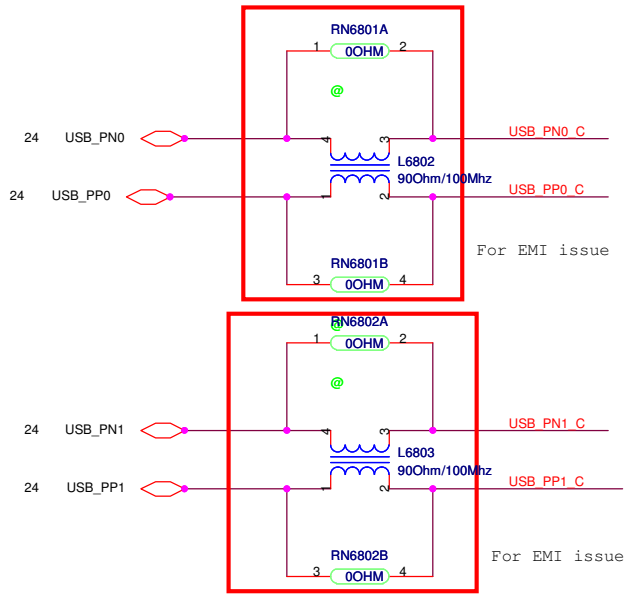
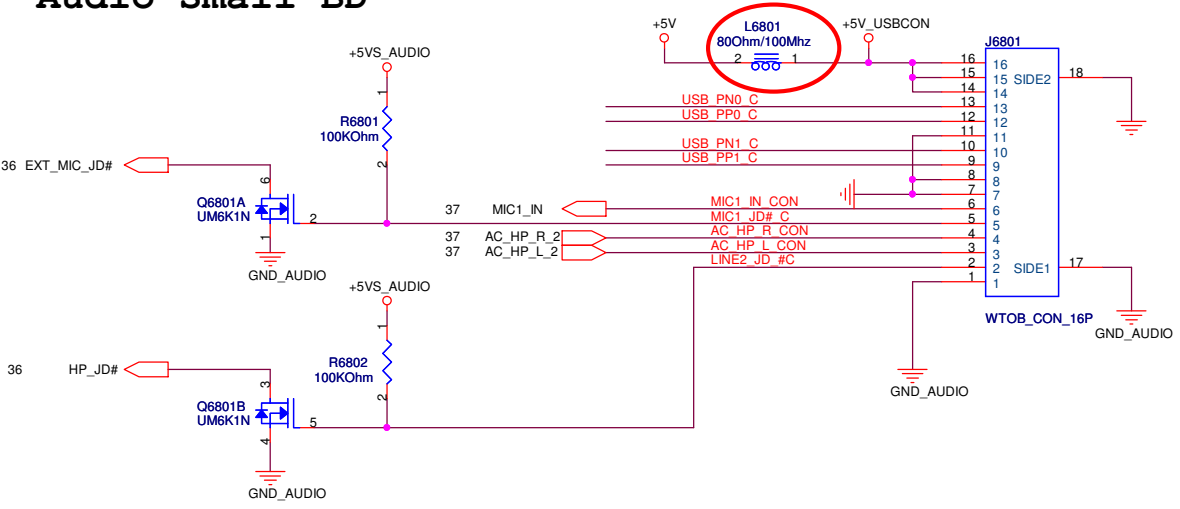
www.aitech1.ru

PEGATRON		Title : PWR SW BD	
Engineer: Jenny_Du			
Size A	Project Name H54FE		Rev 1.1
Date: Friday, May 14, 2010		Sheet 66	of 99

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PEGATRON		Title : HDMI_ESATA COMBO BD	
Engineer: Jenny_Du			
Size A	Project Name H54FE		Rev 1.1
Date: Friday, May 14, 2010		Sheet 67 of 99	

Audio Small BD

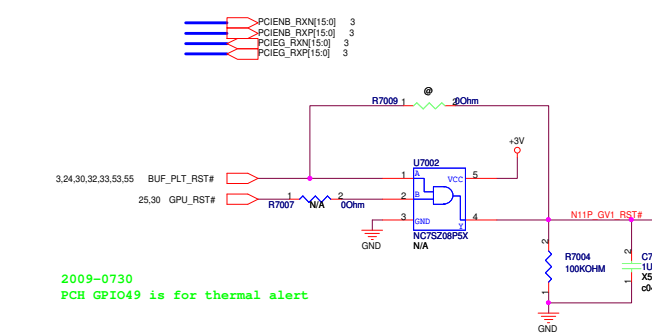


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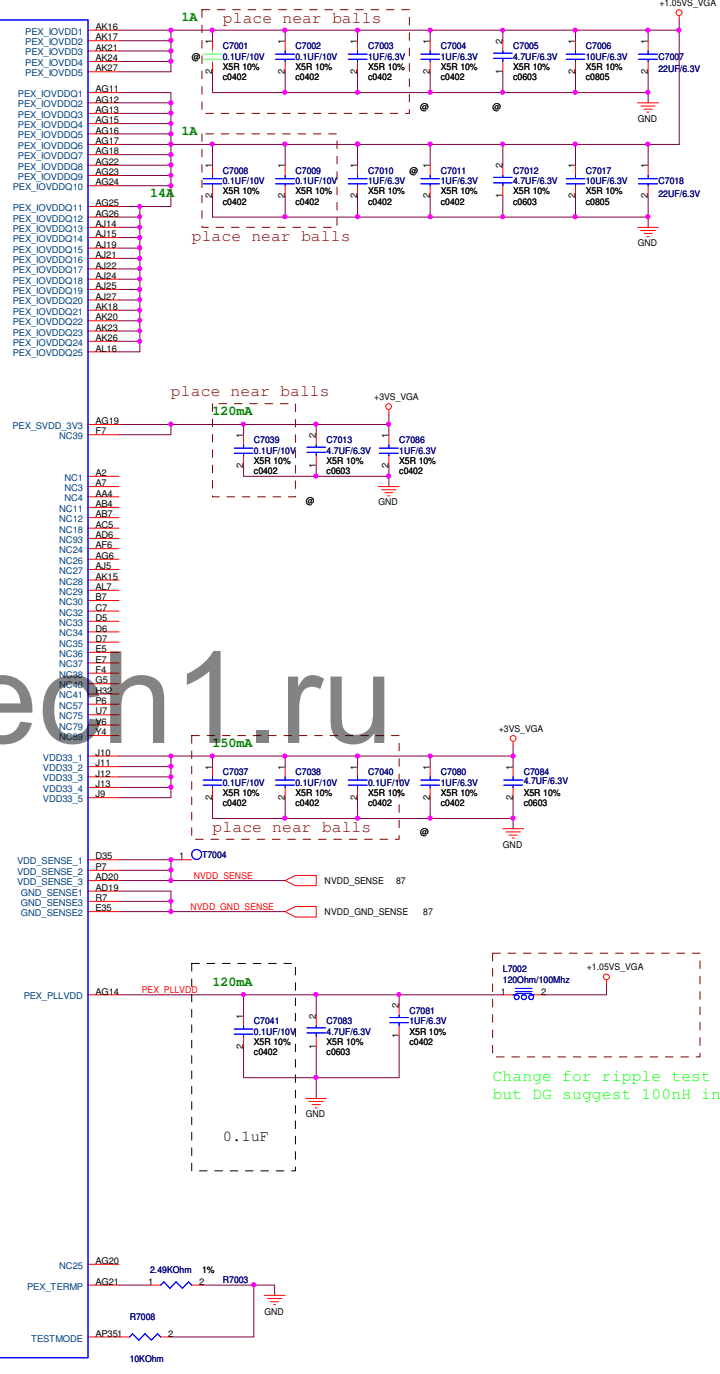
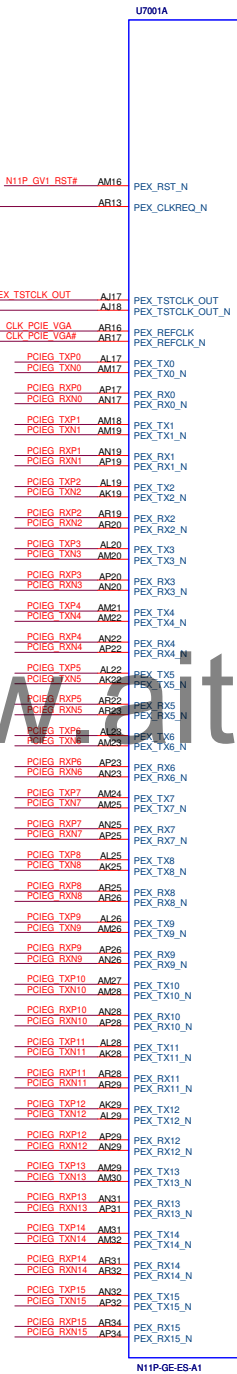
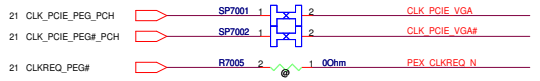
PEGATRON		Title : AUD/USB_BD	
		Engineer: Jenny_Du	
Size B	Project Name H54FE		Rev 1.1
Date: Friday, May 14, 2010		Sheet	69 of 99

Pin compatible list: 20091126
N11P-GE1 -->CUPID BOM USE
N11P-GS1 -->CUPID Schematic USE
N11P-GV1 -->H54F BOM USE



2009-0730
PCH GPIO49 is for thermal alert

PCIEB_RXN15	C7045	1	2	0.1UF/16V	PCIEG_TXN15
PCIEB_RXP15	C7046	1	2	0.1UF/16V	PCIEG_TXP15
PCIEB_RXN14	C7047	1	2	0.1UF/16V	PCIEG_TXN14
PCIEB_RXP14	C7048	1	2	0.1UF/16V	PCIEG_TXP14
PCIEB_RXN13	C7049	1	2	0.1UF/16V	PCIEG_TXN13
PCIEB_RXP13	C7050	1	2	0.1UF/16V	PCIEG_TXP13
PCIEB_RXN12	C7051	1	2	0.1UF/16V	PCIEG_TXN12
PCIEB_RXP12	C7052	1	2	0.1UF/16V	PCIEG_TXP12
PCIEB_RXN11	C7053	1	2	0.1UF/16V	PCIEG_TXN11
PCIEB_RXP11	C7054	1	2	0.1UF/16V	PCIEG_TXP11
PCIEB_RXN10	C7055	1	2	0.1UF/16V	PCIEG_TXN10
PCIEB_RXP10	C7056	1	2	0.1UF/16V	PCIEG_TXP10
PCIEB_RXN9	C7057	1	2	0.1UF/16V	PCIEG_TXN9
PCIEB_RXP9	C7058	1	2	0.1UF/16V	PCIEG_TXP9
PCIEB_RXN8	C7059	1	2	0.1UF/16V	PCIEG_TXN8
PCIEB_RXP8	C7060	1	2	0.1UF/16V	PCIEG_TXP8
PCIEB_RXN7	C7061	1	2	0.1UF/16V	PCIEG_TXN7
PCIEB_RXP7	C7062	1	2	0.1UF/16V	PCIEG_TXP7
PCIEB_RXN6	C7063	1	2	0.1UF/16V	PCIEG_TXN6
PCIEB_RXP6	C7064	1	2	0.1UF/16V	PCIEG_TXP6
PCIEB_RXN5	C7065	1	2	0.1UF/16V	PCIEG_TXN5
PCIEB_RXP5	C7066	1	2	0.1UF/16V	PCIEG_TXP5
PCIEB_RXN4	C7067	1	2	0.1UF/16V	PCIEG_TXN4
PCIEB_RXP4	C7068	1	2	0.1UF/16V	PCIEG_TXP4
PCIEB_RXN3	C7069	1	2	0.1UF/16V	PCIEG_TXN3
PCIEB_RXP3	C7070	1	2	0.1UF/16V	PCIEG_TXP3
PCIEB_RXN2	C7071	1	2	0.1UF/16V	PCIEG_TXN2
PCIEB_RXP2	C7072	1	2	0.1UF/16V	PCIEG_TXP2
PCIEB_RXN1	C7073	1	2	0.1UF/16V	PCIEG_TXN1
PCIEB_RXP1	C7074	1	2	0.1UF/16V	PCIEG_TXP1
PCIEB_RXN0	C7075	1	2	0.1UF/16V	PCIEG_TXN0
PCIEB_RXP0	C7076	1	2	0.1UF/16V	PCIEG_TXP0



other CAPS place near VGA

place near balls

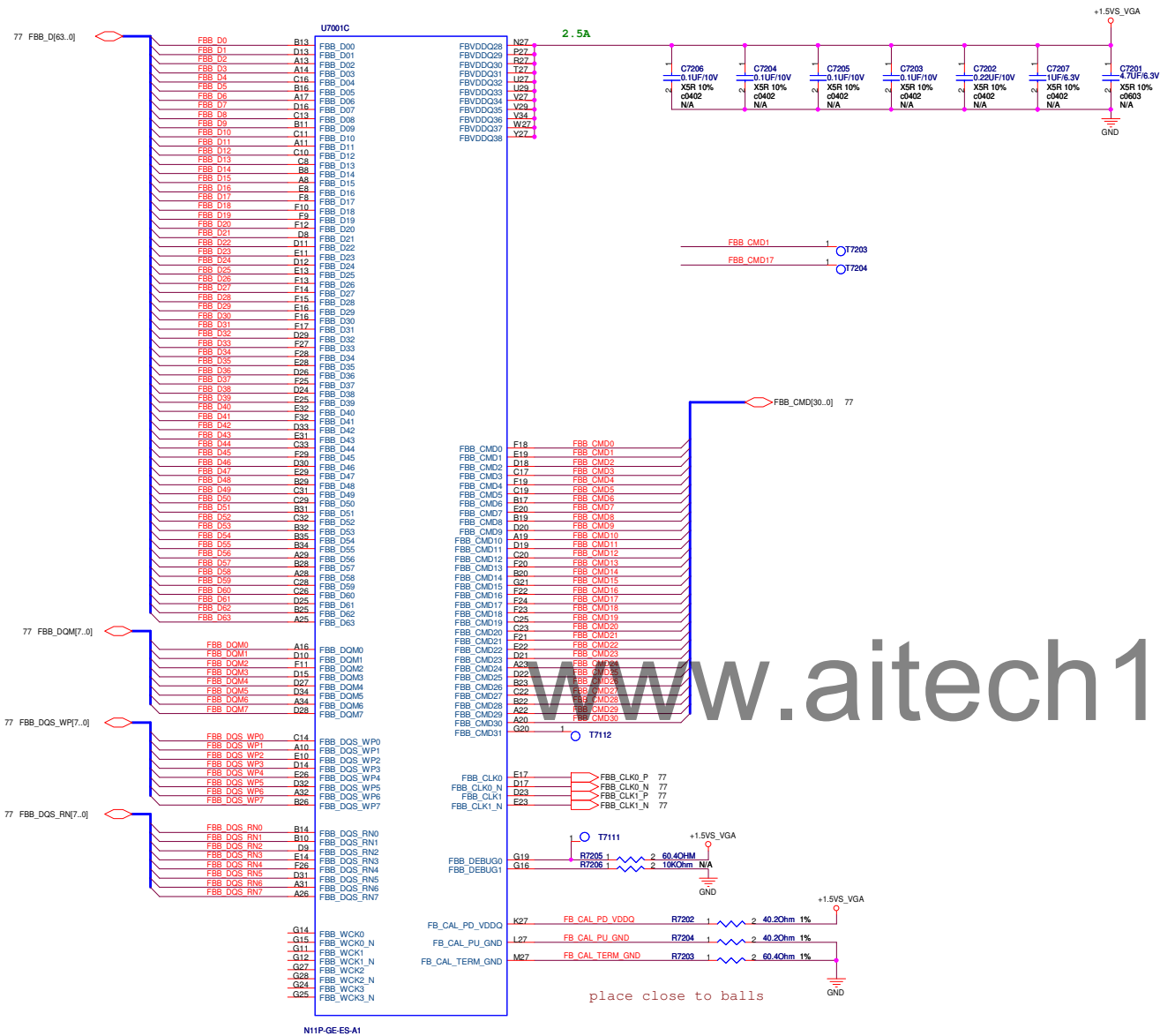
place near balls

place near balls

place near balls

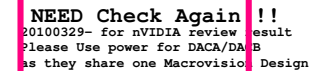
0.1uF

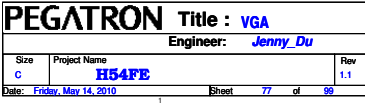
Change for ripple test fail
but DG suggest 100nH inductor



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DEL ON ER





GT21x	0..31	32..63
CMD0	ODT	
CMD1	CS1	
CMD2	CS0	
CMD3	CKE	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS	RAS
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS	CAS
CMD16		CKE
CMD17		CS1
CMD18		CS0
CMD19		ODT
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE	A10
CMD29	BA0	BA0
CMD30	A15	BA2
DEBUG		

Table 5.4 Mode E Command Mapping

N11x Ferret DDR3 mode E	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT	
FBx_CMD1	CS1*	
FBx_CMD2	CS0*	
FBx_CMD3	CKE	
FBx_CMD4	A9	A11
FBx_CMD5	A6	A7
FBx_CMD6	A3	BA1
FBx_CMD7	A0	A12
FBx_CMD8	A8	A8
FBx_CMD9	A12	A0
FBx_CMD10	A1	A2
FBx_CMD11	RAS*	RAS*
FBx_CMD12	A13	A14
FBx_CMD13	BA1	A3
FBx_CMD14	A14	A13
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CKE
FBx_CMD17		CS1*
FBx_CMD18		CS0*
FBx_CMD19		ODT
FBx_CMD20	RST	RST
FBx_CMD21	A7	A6
FBx_CMD22	A4	A5
FBx_CMD23	A11	A9
FBx_CMD24	A2	A1
FBx_CMD25	A10	WE*
FBx_CMD26	A5	A4
FBx_CMD27	BA2	A15
FBx_CMD28	WE*	A10
FBx_CMD29	BA0	BA0
FBx_CMD30	A15	BA2
FBx_CMD31		

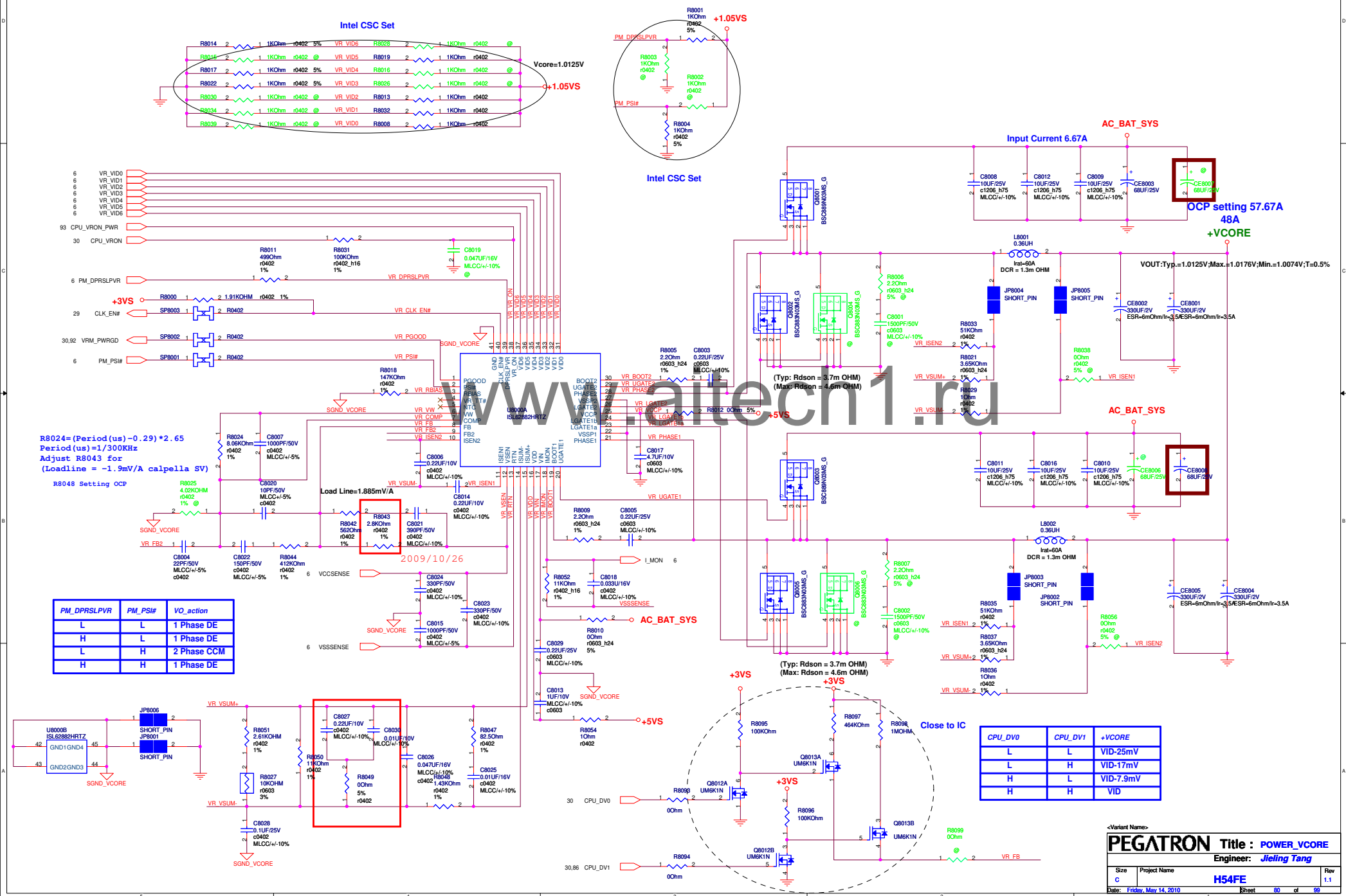
H54FE_R10_Changelist_2010-04-06

- 1 . Add DDR3 VRAM.....P76,P77
- 2. Reserve GPU_RST to GPU.....P70
- 3. Add USB3.0.....P55,P24
- 4. Add PCH sink NUT.....P65
- 5. Change Discrete to Optimus.....P74,P75
- 6. Delete All Discrete Display except for CRT.....P45
- 7. Delete Dicrete reserve display.....P46,P48
- 8. Change RTC Connector to flat type.....P20

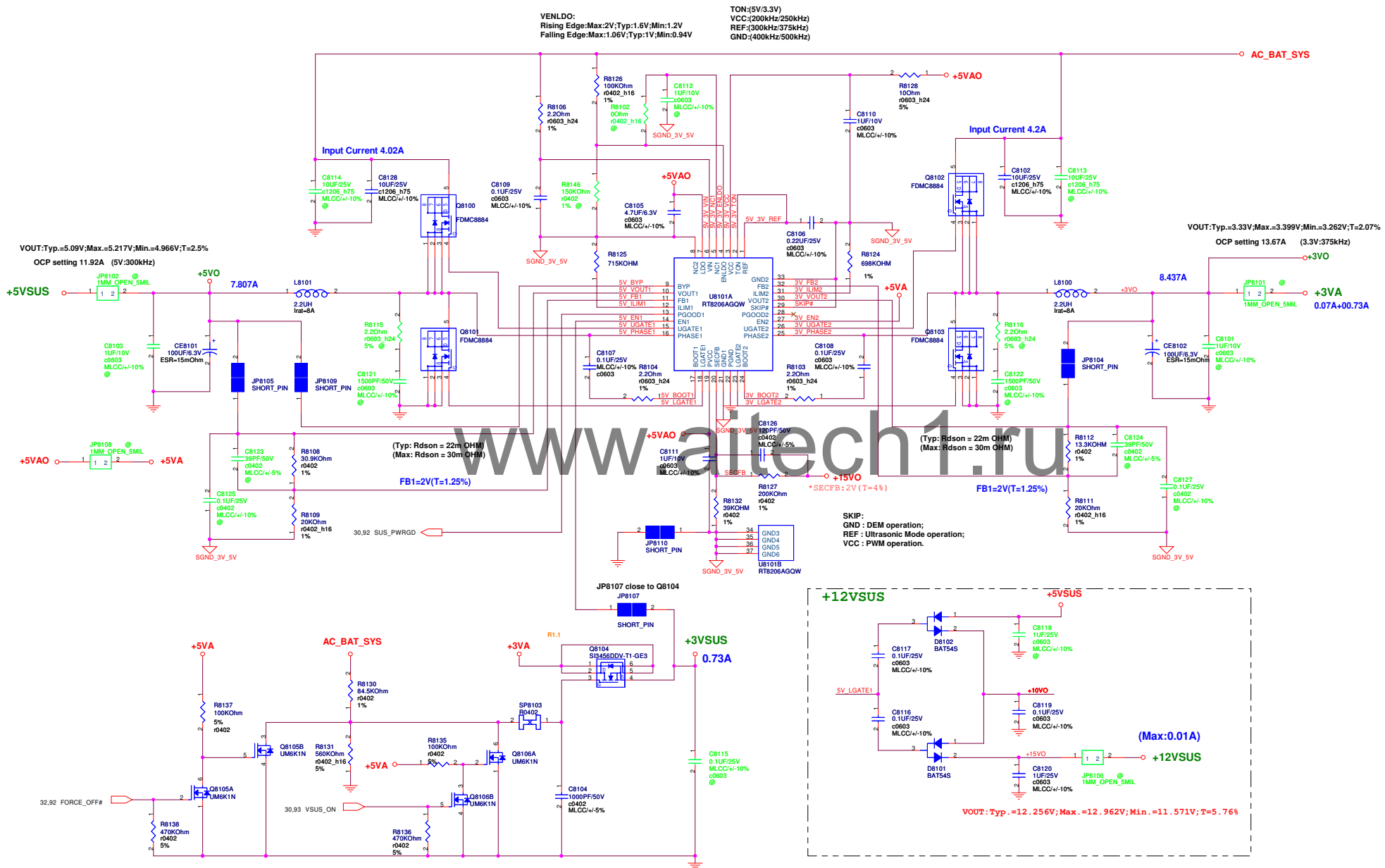
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PEGATRON		Title : HISTORY	
BG1/RD3		Engineer: Jenny_Du	
Size	Project Name		Rev
A	H54FE		1.1
Date: Friday, May 14, 2010		Sheet	79 of 99

IMVP6.5 CPU VCORE REGULATOR



+5V / +3.3V POWER SUPPLY



<Variant Name>

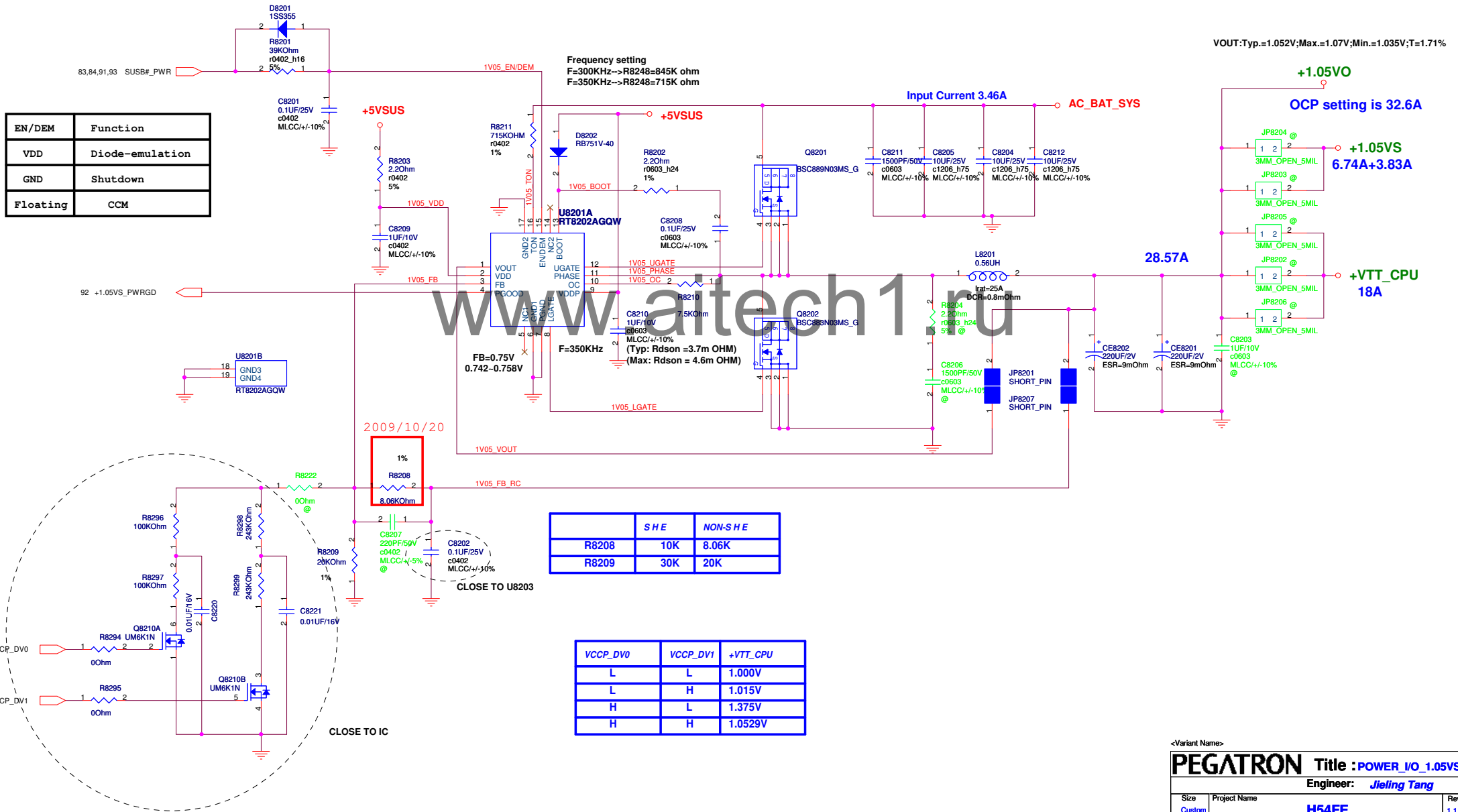
PEGATRON Title :POWER_SYSTEM

Engineer: **Jieling Tang**

Size	Project Name	Rev
Custom	H54FE	1.1

Date: Friday, May 14, 2010 Sheet 81 of 99

+VTT_CPU & +1.05VS POWER SUPPLY

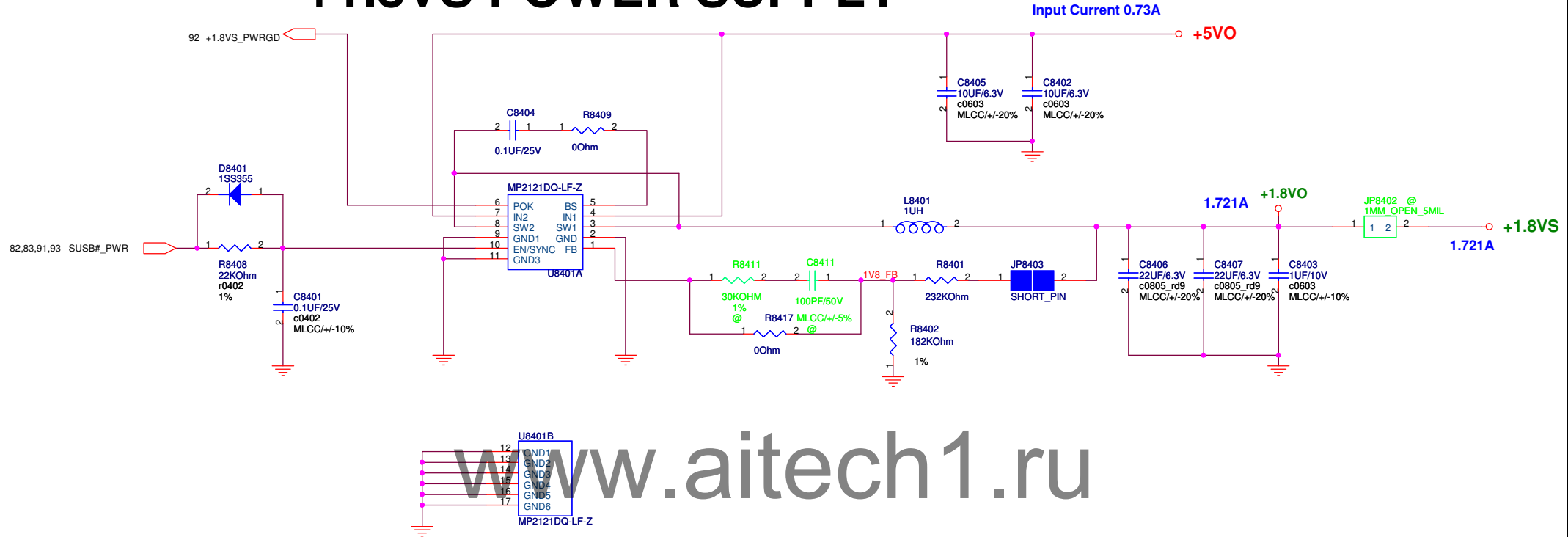




Engineer: *Jieling Tang*

Date: Friday, May 14, 2010 Sheet 83 of 99

+1.8VS POWER SUPPLY



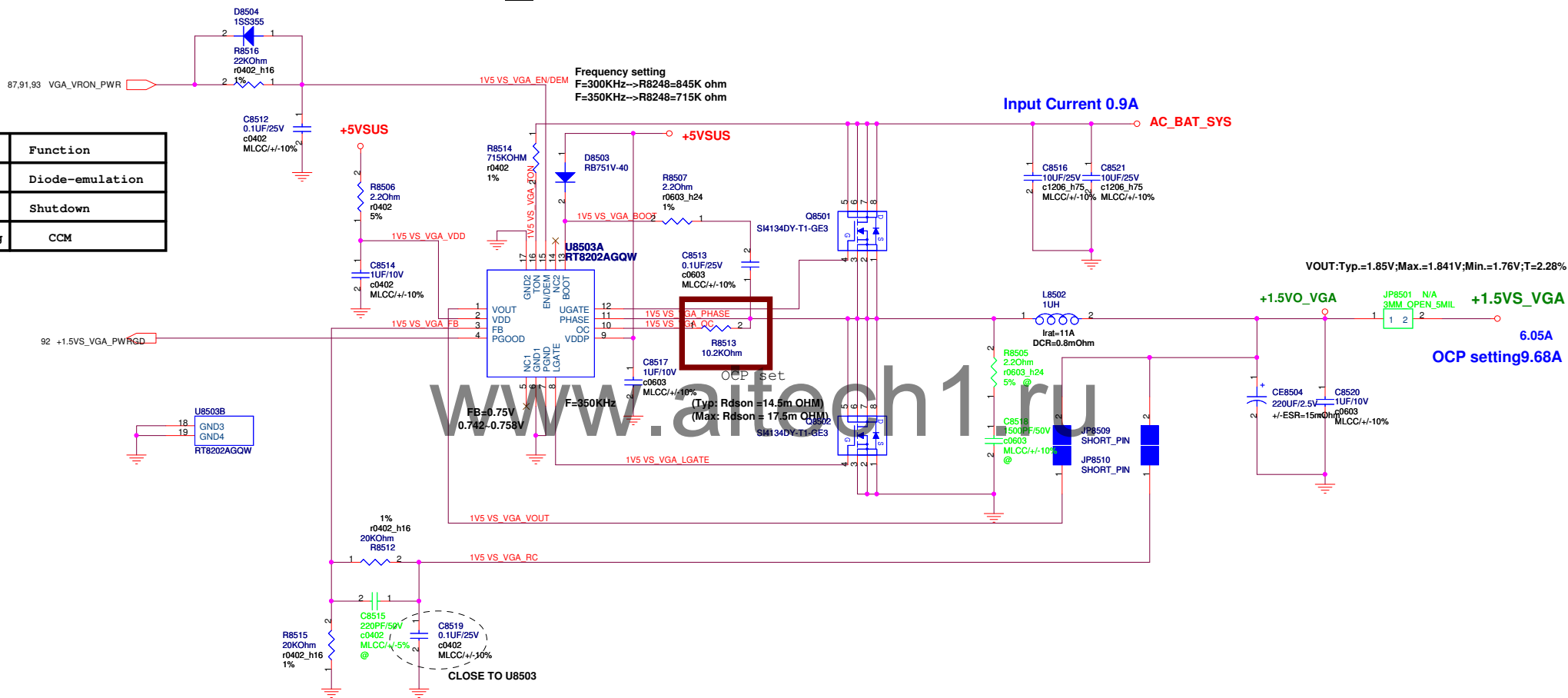
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<Variant Name>

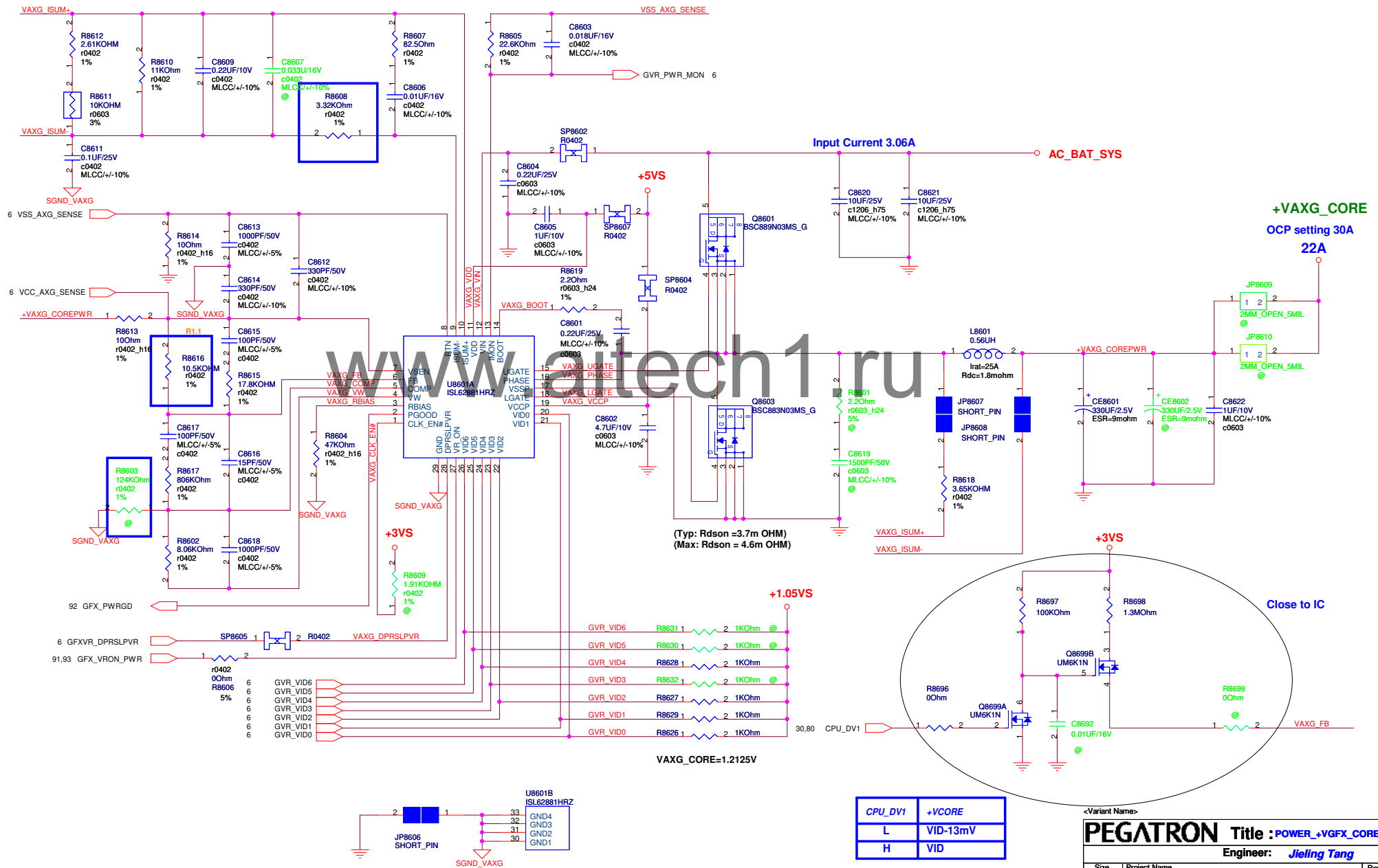
PEGATRON			Title :POWER_+1.8VS
Engineer:			Jielling Tang
Size	Project Name	Rev	
B	H54FE	1.1	
Date: Friday, May 14, 2010		Sheet	84 of 99

+1.5VS_VGA POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



+VAXG_CORE POWER SUPPLY



75 GPU_VID2

75 GPU_VID1

75 GPU_VID0

VGA CORE=0.95V

	0.85V	0.9V	0.95V
GPU_VID2	1	1	0
GPU_VID1	0	0	1
GPU_VID0	1	0	1

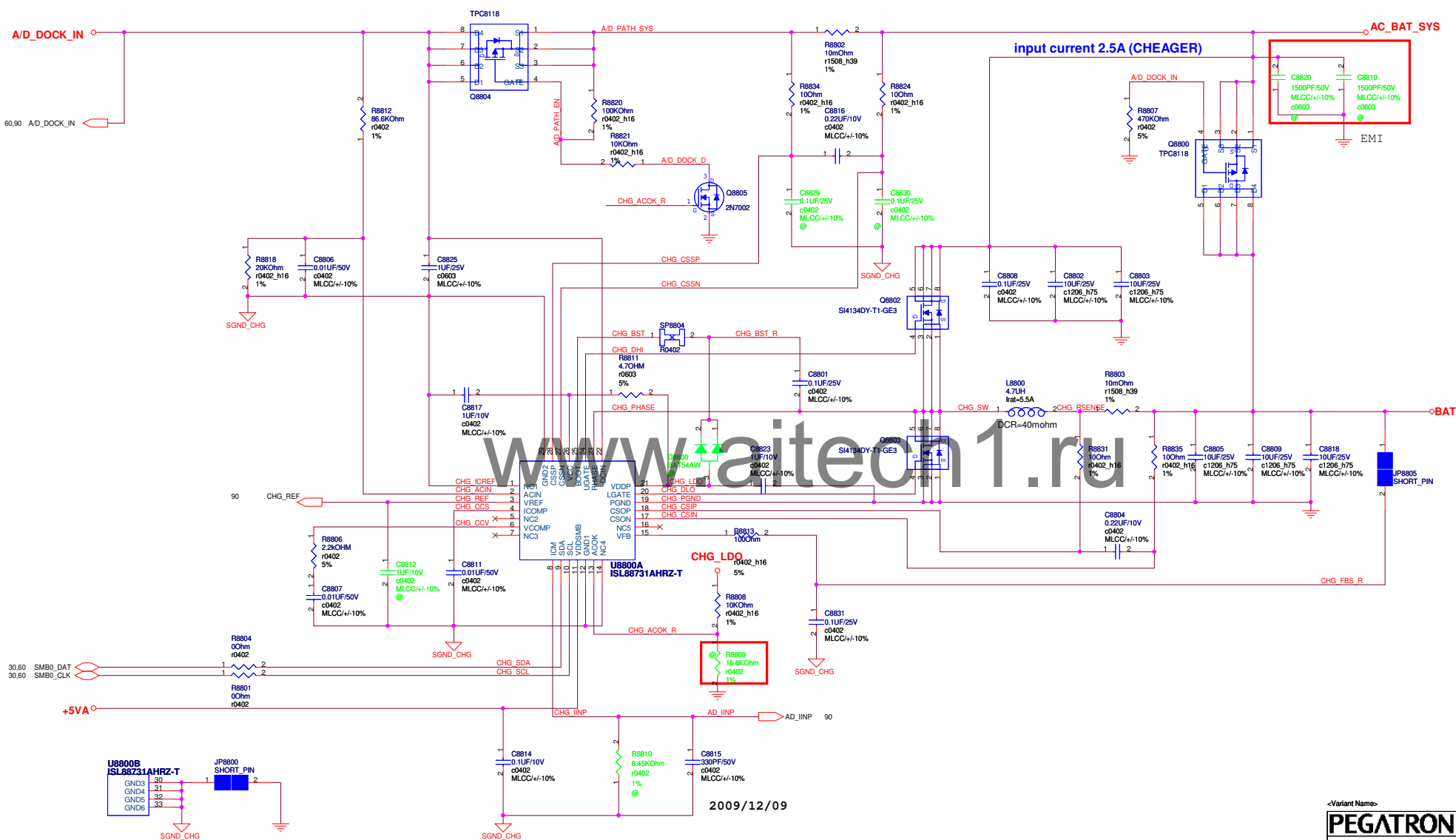
```
R8024=(Period(us)-0.29)*2.65
Period(us)=1/300KHz
Adjust R8043 for
(Loadline = -1.9mV/A calpella SV)
```

R8048 Setting OCP

<i>PM_DPRSLPVR</i>	<i>PM_PSI#</i>	<i>VO_action</i>
L	L	1 Phase DE
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

PEGATRON						Title :	POWER_VCORE
Engineer: <i>Jieling Tang</i>							
Size C	Project Name					H54FE	R 1.
Date: Friday, May 14, 2010			Echant		R7	nl	99

BATTERY CHARGER



2009/12/09

<Variant Name>

PFGATRON Title : **POWER CHARGER**

Engineer: **Jieling Tang**

Size Custom	Project Name H54FE	Rev 1.1
Date: Friday, May 14, 2010	Sheet 88 of 99	

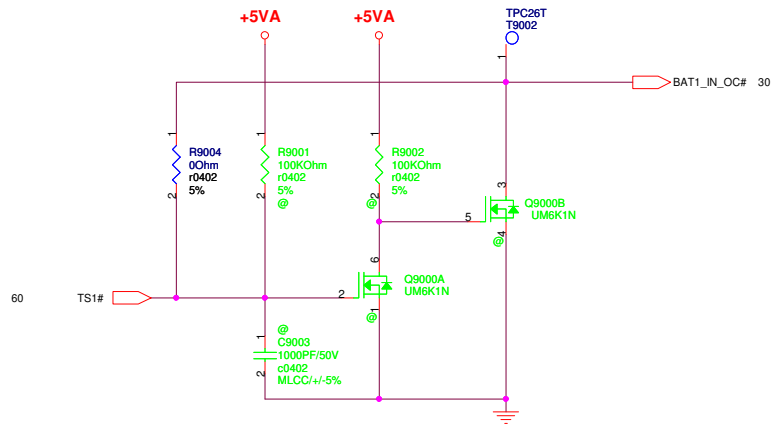
Custom	11941 E		
Date:	Friday, May 14, 2010	Shoot	88 of 88

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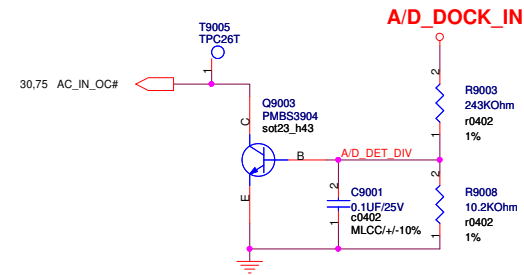
<Variant Name>

PEGATRON		Title : POWER_NA	
Engineer: Jieling Tang			
Size A	Project Name H54FE		Rev 1.1
Date: Friday, May 14, 2010		Sheet	89 of 99

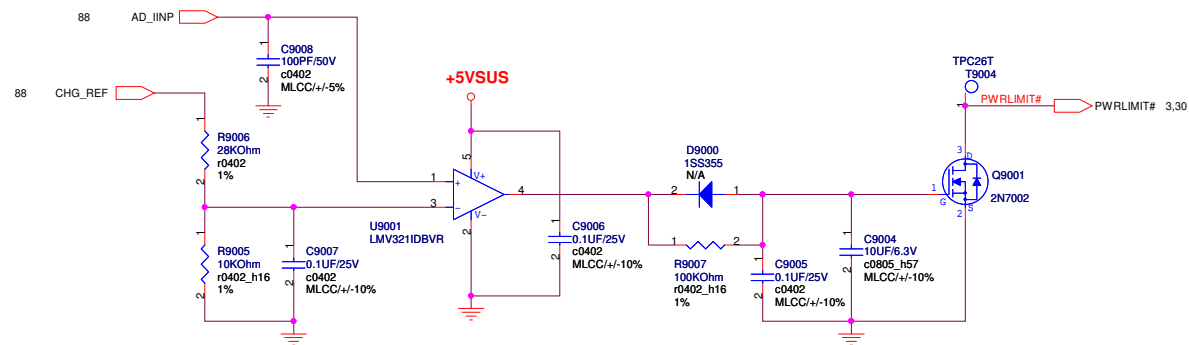
BATTERY IN DETECT



ADAPTER IN DETECT



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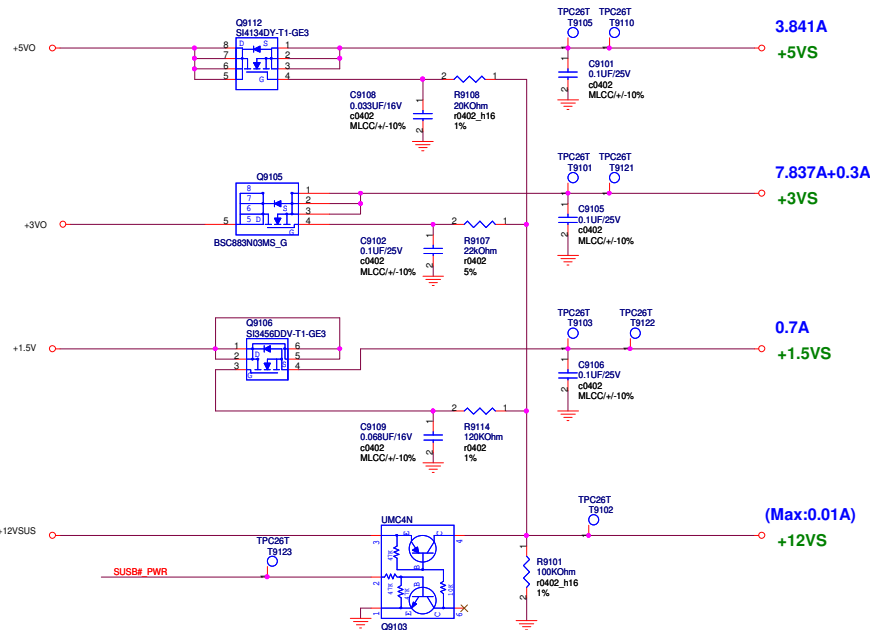
Pinput=83W---->Iinput=4.368A
R8802=10mohm
Vicm=20*Iinput*R8802 ==> Vicm=0.87V

<Variant Name>

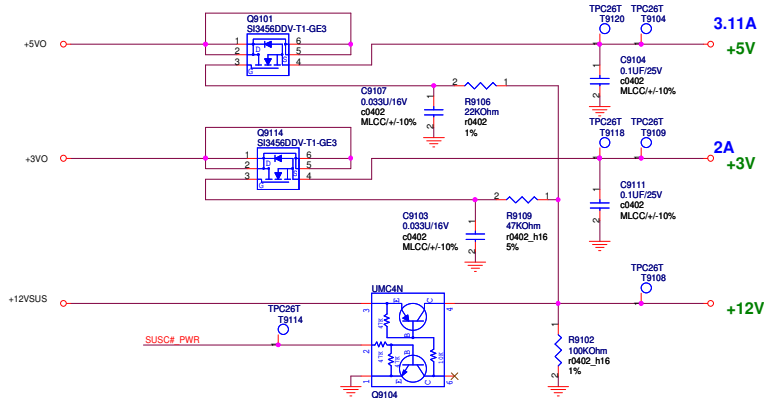
PEGATRON Title :POWER_DETECT
Engineer: Jieling Tang

Size	Project Name	Rev
Custom	H54FE	1.1
Date: Friday, May 14, 2010	Sheet 90 of 99	

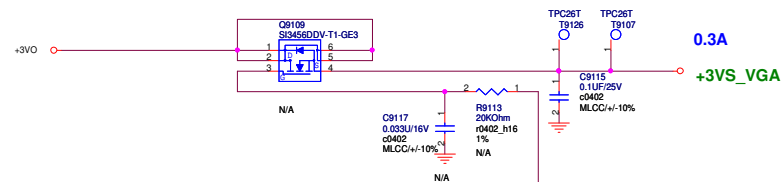
SUSB#_PWR_LOAD_SW



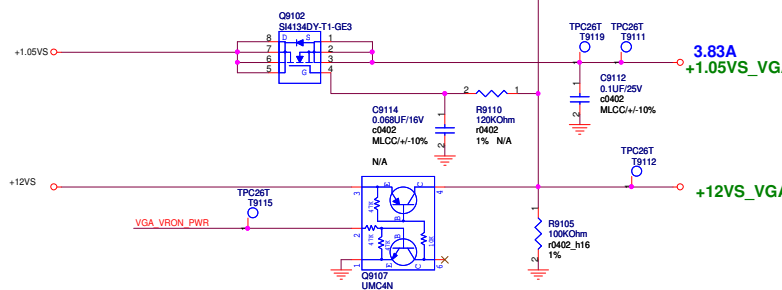
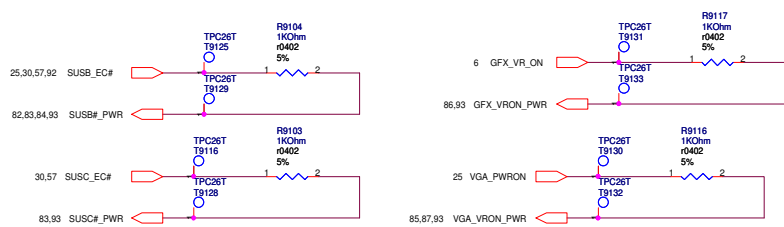
SUSC# PWR LOAD SW



VGA_PWR LOAD SW

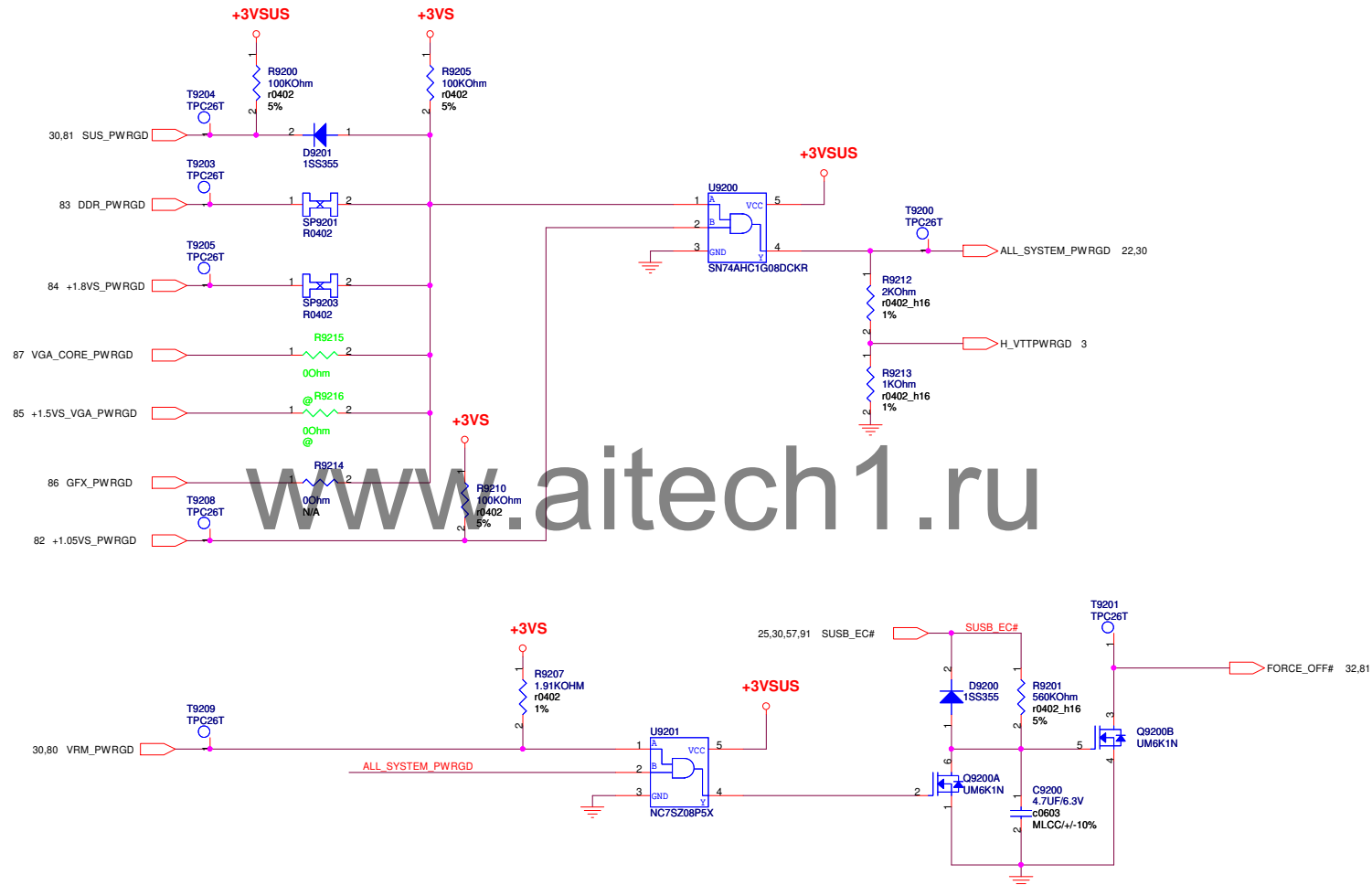


ENABLE SINGAL



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POWER GOOD DETECTOR



<Variant Name>

PEGATRON Title : **POWER_PROTECT**
 Engineer: **Jieling Tang**

Size	Project Name	Rev
Custom	H54FE	1.1
Date: Friday, May 14, 2010	Sheet 92 of 99	

AC_BAT_SYS AC_BAT_SYS 45,80,81,82,83,85,86,87,88
BAT BAT 60,88

+3VA +3VA 20,30,56,57,81
+5VAO +5VAO 81
+5VA +5VA 56,81,88,90

+5VO +5VO 81,84,91
+3VO +3VO 81,91
+1.8VO +1.8VO 84
+0.75VO +0.75VO 83
+1.05VO +1.05VO 82

+1.5VO +1.5VO 83
+5VSUS +5VSUS 27,56,81,82,83,85,90
+3VSUS +3VSUS 21,22,24,25,27,30,33,34,81,92
+12VSUS +12VSUS 28,81,91

+5V +5V 36,52,55,56,57,68,87,91
+3V +3V 24,40,53,55,57,61,70,91
+12V +12V 91

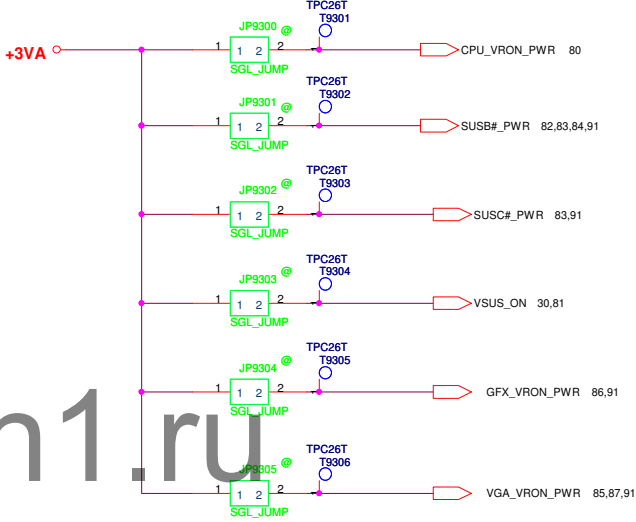
+3VS +3VS 3,7,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,44,45,46,48,50,51,53,54,56,57,80,86,87,91,92
+5VS +5VS 27,30,31,36,46,48,50,51,54,56,57,80,86,87,91
+12VS +12VS 28,48,91
+1.05VS +1.05VS 26,27,29,57,80,82,86,91
+1.05VS_VGA +1.05VS_VGA 57,70,71,73,91
+1.5VS +1.5VS 53,57,91
+0.75VS +0.75VS 16,17,18,57,83
+1.8VS +1.8VS 6,26,57,84
+1.5VS_VGA +1.5VS_VGA 25,57,71,72,76,77,85

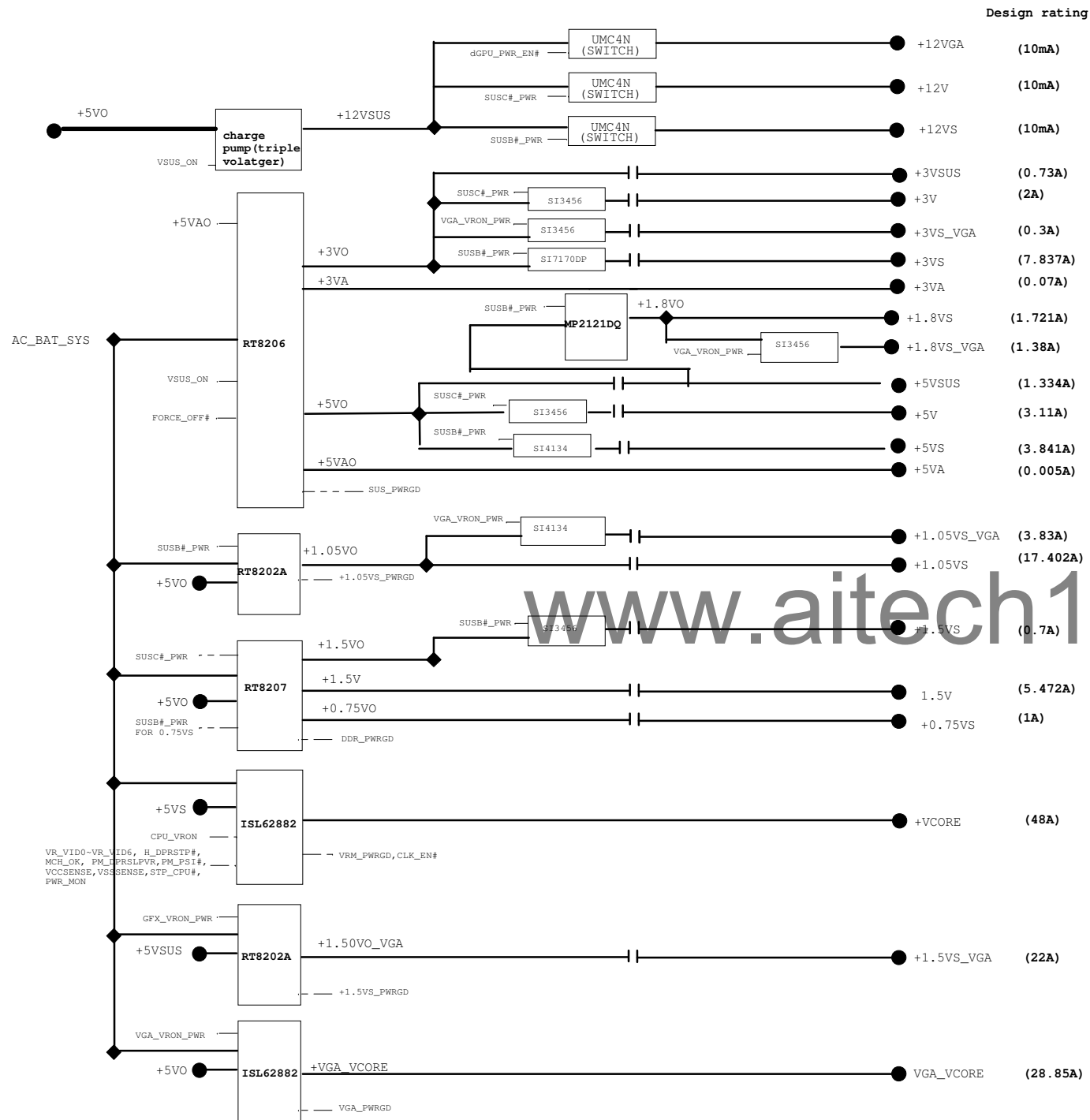
+VCORE +VCORE 6,57,80

+VAXG_CORE +VAXG_CORE 6,57,86

+VGA_VCORE +VGA_VCORE 57,73,87

FOR POWER TEST





Design rating

(10mA)
(10mA)
(10mA)
(0.73A)
(2A)
(0.3A)
(7.837A)
(0.07A)
(1.721A)
(1.38A)
(1.334A)
(3.11A)
(3.841A)
(0.005A)
(3.83A)
(17.402A)
(0.7A)
(5.472A)
(1A)
(48A)
(22A)
(28.85A)

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- R1.0
2. change Q9105 from SI4134 to SI7170 ,and later to BSC883 for load increased.....P91
 3. change L8100 and L8101 from 3.3u to 2.2u for load increased.....P81
 4. change the net 1.8VS_PWRGD in the page 85 to 1.5VS_PWRGD.....P85
 5. change the VGA_CORE VID for the output fixed 0.9VP87.
 6. Add net +1.5VS_PWRGD.....P92
 7. Add Q9107 and R9105 for VGA_PWR LOAD SW.....P91
 8. Add POWER LIMIT CIRCUITP90
 9. change the R8210 from 4.12Kohm to 7.5Kohm for OCP setting.....P82
 10. change the R8125 from 300Kohm to 715Kohm for OCP setting.....P81
 11. change the R8124 from 322Kohm to 820Kohm for OCP setting.....P81
 12. add +VAXG_CORE SWITCH circuit and later delete.....P83
 13. add VGA_PWR LOAD SW and delete JP8316 and JP8314.....P83
 14. add Super Hybrid Engine circuit.....P80,P82,P86
 15. add 86_POWER_+VAXG_CORE circuit instead the FIXED 1.5V +VAXG_CORE circuit.....P86
 16. add JP9305 and JP9304 for PWR test.....P93
 17. add R9214 and 9215 for POWER PROTECT.....P92
 18. delete Q9110,R9115,C9116,C9118 for there is no load for +1.8VS_VGA.....P91
 19. change the R8513 from 24.9ohm to 3.6Kohm for OCP setting.....P85
 20. change R8608 from 2.32Kohm to 3.32Kohm AND change R8616 from 8.45Kohm to 10.5Kohm for OCP and loadline setting.....P86
 21. change R8603 from 249Kohm to 124Kohm for OCP and IC function setting AND reserved.....P86
 22. add Super Hybrid Engine circuit in VGA_CORE.....P87
 23. change the net +5VSUS input for Q9112 and Q9101 to +5VO to make LAYOUT easier.....P91
 24. delete the net BAT_COM for there is no connection for it.....P93
 25. change the R8302 from 8.45Kohm to 28Kohm for OCP setting.....P83
 26. change the R8513 from 3.6Kohm to 10.2Kohm for OCP setting.....P85
 27. change the Q8302,Q8301,8501,8502,Q8802,8803 from SI4336+SI4392,BSC889+BSC883, IRF8707+IRF8707 TO SI4134.....P83,P85,P88
 28. change the CE8301,CE8302,CE8504 from 330UF to 220UFP83,P85
 29. change the CE8701,CE8702 from 330UF to 220UFP87
 30. change the R8411,C8411,R8402 from 0603 size to 0402 for making Layout easierP84
 31. change the C8603 from 0.22UF to 0.018UF for Imon settingP86
 32. change the VAXG VID from 0100110 to 0010111P86
 33. make the R8609 reserved for VAXG_CLK_EN# does not connect to EE.....P86

R1.1

2. change GPU VID pull high net from +1.05VS to +3VS FOR NV GPU VID is 3V.....P87
3. Q8301, Q8302 to SI4134 to USE the PWR pad package.....P87
4. add VGA_CORE_PWRGD circuitP87
5. change R8124 to 698K for OCP settingP81
6. change R8704 from 2.8K to 1.43K ohm.....P87
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